Problem: CM5 **Area: Integrated Circuits and Logic Design** **Code #_____**

Given the Boolean expression, answer the following questions:

$$F(A,B,C) = \overline{(A + \overline{BC})}(\overline{A} + B + \overline{C})(A + \overline{B} + C) + \overline{B}$$

a) Find the truth table for F.

b) Simplify the function F using any appropriate method (express F in its simplest form).

Problem: CM6 **Area: Integrated Circuits and Logic Design** **Code #_____**

Given the state table below with the state variables X and Y, externally applied input r, and output g. Answer the questions below.

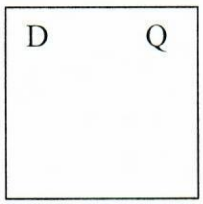
Present Input	Present State		Present Output	Next State		JK Flip Flop Inputs		SR Flip Flop Inputs	
r	X	Y	g	X*	Y*	J_X	K_X	S_Y	R_Y
0	0	0	0	0	1				
0	0	1	0	1	0				
0	1	0	1	0	0				
0	1	1	0	0	1				
1	0	0	1	1	0				
1	0	1	1	1	1				
1	1	0	0	0	1				
1	1	1	0	1	1				

a) Fill in the missing values for the state table.
b) Draw the state transition diagram based on the state table.

Problem: CM7 **Area: Integrated Circuits and Logic Design** **Code #_____**

Make a JK flip-flop out of the D flip-flop below. Show all your work and draw the resulting circuit.

J	K	Q	Q*	D
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		



Problem: CM8 **Area: Integrated Circuits and Logic Design** **Code #_____**

Given the function: $F(w,x,y,z) = \sum(0,1,2,3,5,7,9,12)+dc(4,10,111)$

Answer the following questions.

a) Write the minimal sum-of-product expression for F.

wx \ yz	00	01	11	10
00				
01				
11				
10				

b) Write the minimal product-of-sums expression for F.

wx \ yz	00	01	11	10
00				
01				
11				
10				

c) Write the minimal NAND-NAND expression for F.

wx \ yz	00	01	11	10
00				
01				
11				
10				

Problem: CM9 **Area: Embedded Computer Systems** **Code #_____**

a) Describe addressing modes used by 8051 instructions set

b) Describe basic memory organization used in 8051 micro-controllers. What types of memory exist and how are they used, accessed, and mapped?

Problem: CM10 **Area: Embedded Computer Systems** **Code #_____**

Consider the following WIMP51 (simplified 8051) assembly program.

Address	Label	Instruction	Binary code	Hex code
00H		MOV A, #04H		
		MOV R1, A		
		MOV A, #B2H		
		MOV R0, A		
		CLR C		
	Loop:	MOV A, #01H		
		ADDC A, R0		
		MOV R0, A		
		ANL A, R1		
		JZ Loop		
	Stop:	SJMP Stop		

a) Fill the table above (the **machine code in binary code and hex code**) for this program using the summary of WIMP51 Inst Set shown below. For each machine code instruction, **determine its address** as well. Assume that the beginning address of the program is 00H.

Summary of WIMP51 Inst Set

ASM code	Machine code	Meaning
MOV A, #D	01110100 dddddddd	A<=D
ADDC A,#D	00110100 dddddddd	C,A<=A+D+C
MOV Rn, A	11111nnn	Rn<=A
MOV A, Rn	11101nnn	A<=Rn
ADDC A, Rn	00111nnn	C,A<=A+Rn+C
ORL A, Rn	01001nnn	A<=A OR Rn
ANL A, Rn	01011nnn	A<= A AND Rn
XRL A, Rn	01101nnn	A<=A XOR Rn
SWAP A	11000100	$A<=A_{(3-0)}\&A_{(7-4)}$
CLR C	11000011	C<=0
SETB C	11010011	C<=1
SJMP rel	10000000 aaaaaaaa	PC<=PC+rel+2
JZ rel	01100000 aaaaaaaa	PC<=PC+rel+2 if Z=1

b) How long does it take to execute this program in **clock cycles**? **Note:** Write the assumptions (machine cycle length, instruction cycle length).

c) List all registers that are used by this program (PC, ACC, Z, R0, and R1) and list their contents after each instruction is executed.

Instruction Cycle #	PC	ACC	Z	R0			
0	00h	X	X	X			
1							
2							
3							
4							
5							
6							
7							
8							
9							
10							
11							

Problem: CM11 **Area: Embedded Computer Systems** **Code #_____**

a) Identify at least 3 differences between general-purpose microprocessors and microcontrollers and discuss why these differences exist.

b) Discuss advantages and disadvantages of programming microcontrollers in assembly language instead of C/C++.

Problem: CM12 **Area: Embedded Computer Systems** **Code #_____**

Consider a timer 0 in 8051 type processor with hardware configuration and control registers shown on the attached figures and tables (see next pages). Assume following: SYSCLOCK = 12MHz, External Clock (T0) = 1MHz

a) Explain how the timer 0 operates in Mode 2 (timer/counter with auto-reload).

b) Consider that the timer should overflow (timeout) every 1ms. Which clock source can you use to achieve this timeout: SYSCLK or External Clock (T0)? What reload value should be used? **Note**: The SYSCLK signal can be pre-scaled before driving the timer (slowed down).

c) Write a short assembly or embedded C code that setups the timer 0 to generate interrupt every 1ms. Make sure only the corresponding bits are modified.

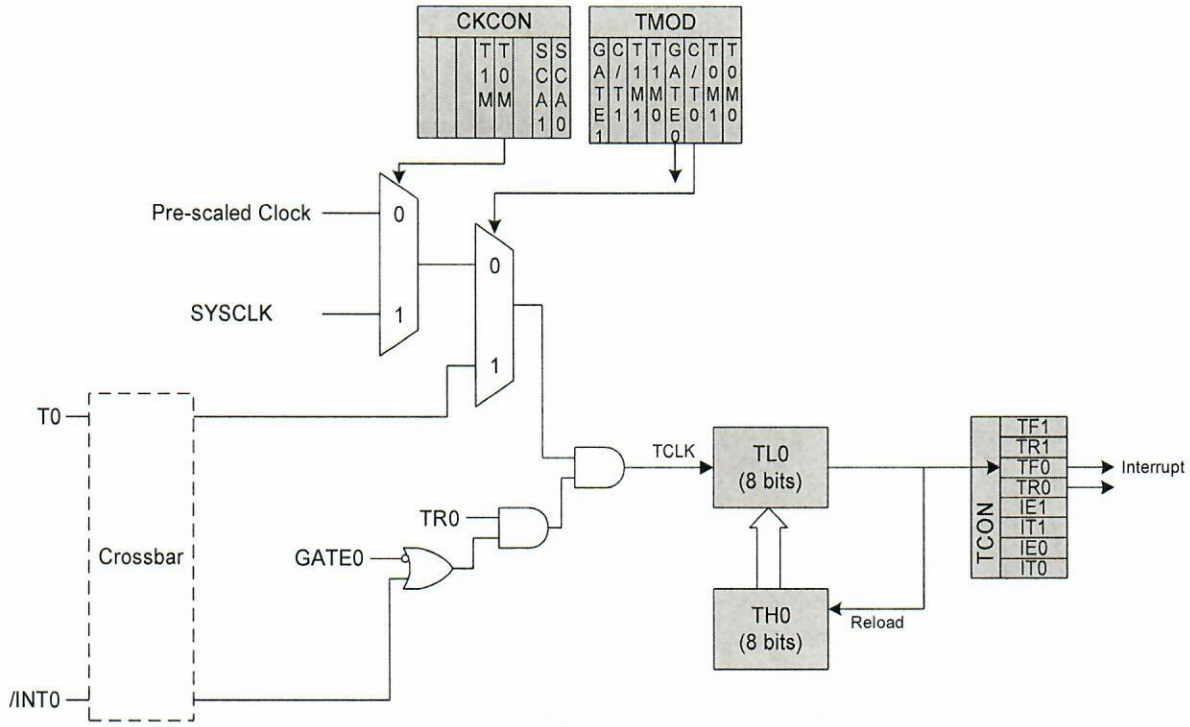


Figure 23.2. T0 Mode 2 Block Diagram

SFR Definition 23.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x89
SFR Page: 0

Bit7: GATE1: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of /INT1 logic level.
1: Timer 1 enabled only when TR1 = 1 AND /INT1 = logic 1.

Bit6: C/T1: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5–4: T1M1–T1M0: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: GATE0: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of /INT0 logic level.
1: Timer 0 enabled only when TR0 = 1 AND /INT0 = logic 1.

Bit2: C/T0: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1–0: T0M1–T0M0: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

SFR Definition 23.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x88
SFR Page: 0

Bit7: TF1: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 signal.

Bit2: IT1: Interrupt 1 Type Select.
This bit selects whether the configured /INT1 interrupt will be falling-edge sensitive or active-low.
0: /INT1 is level triggered, active-low.
1: /INT1 is edge triggered, falling-edge.

Bit1: IE0: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 signal.

Bit0: IT0: Interrupt 0 Type Select.
This bit selects whether the configured /INT0 interrupt will be falling-edge sensitive or active-low.
0: /INT0 is level triggered, active logic-low.
1: /INT0 is edge triggered, falling-edge.

SFR Definition 23.3. CKCON: Clock Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	T1M	T0M	-	SCA1	SCA0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8E
SFR Page: 0

Bits7–5: UNUSED. Read = 000b, Write = don't care.
Bit4: T1M: Timer 1 Clock Select.
This select the clock source supplied to Timer 1. T1M is ignored when C/T1 is set to logic 1.
0: Timer 1 uses the clock defined by the prescale bits, SCA1–SCA0.
1: Timer 1 uses the system clock.
Bit3: T0M: Timer 0 Clock Select.
This bit selects the clock source supplied to Timer 0. T0M is ignored when C/T0 is set to logic 1.
0: Counter/Timer 0 uses the clock defined by the prescale bits, SCA1-SCA0.
1: Counter/Timer 0 uses the system clock.
Bit2: UNUSED. Read = 0b, Write = don't care.
Bits1–0: SCA1–SCA0: Timer 0/1 Prescale Bits
These bits control the division of the clock supplied to Timer 0 and/or Timer 1 if configured to use prescaled clock inputs.

SCA1	SCA0	Prescaled Clock
0	0	System clock divided by 12
0	1	System clock divided by 4
1	0	System clock divided by 48
1	1	External clock divided by 8*

***Note:** External clock divided by 8 is synchronized with the system clock, and external clock must be less than or equal to the system clock frequency to operate the timer in this mode.

SFR Definition 23.4. TL0: Timer 0 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8A
SFR Page: 0

Bits 7–0: TL0: Timer 0 Low Byte.
The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 23.6. TH0: Timer 0 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8C
SFR Page: 0

Bits 7–0: TH0: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

Problem: CM13 **Area: Computational Intelligence** **Code #_____**

For Deep Learning, why do they call it "deep"? How deep is deep enough to be deep?

Problem: CM14 **Area: Computational Intelligence** **Code #_____**

Compare and contrast, using math and your explanations, normal Q Learning vs. Deep Q learning.

Problem: CM15 **Area: Computational Intelligence** **Code #_____**

Compare and contrast, using math and your explanations, ART1 and Fuzzy ART.

Problem: CM16 **Area: Computational Intelligence** **Code #_____**

Compare and contrast two different major approaches to evolutionary computation.

Problem: CM17 **Area: Networking** **Code _____**

Compare the UDP and TCP protocols in terms of each of the following attributes:

a. bit overhead
b. processing overhead
c. reliability
d. flexibility in supporting different types of traffic, e.g., VoIP, file transfer, telemetry

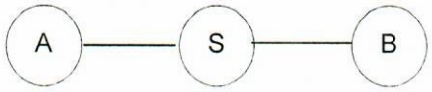
Problem: CM18 **Area: Networking** **Code _____**

Answer <u>all three</u> of the following questions about Cyclic Redundancy Code (CRC).

a. Concisely describe CRC.
b. Discuss the usage of CRC for error detection. Include a description of the relationship between the size of a given CRC code and the number of single-bit errors that it can detect.
c. Discuss the usage of CRC for error correction. Compare this usage its error detection applications.

Problem: CM19 **Area: Networking** **Code _____**

In the network depicted in the figure below, hosts A and B are each connected to a switch, S, via 100 Mbps links. The propagation delay on each link is 20 μs. S is a store-and-forward device; it begins forwarding as soon as it has received a complete frame.



Answer <u>all three</u> questions below. <u>Show every step of your work.</u>

a. Calculate the total time required to transmit a message of 10,000 bits from A to B. The message is sent as a single frame. Assume (unrealistic, but do it) that no header is required for any frame and that processing delay is negligible.
b. Repeat part a, with one change: this time assume the message is transmitted as two 5000-bit frames, sent one right after the other
c. Now consider a change to part b. – we send the message as ten 1000-bit frames instead of two 5000-bit frames. Do you expect the total delay to increase or decrease? No math is expected for this part of the question. You are expected to give an answer in words that show that you understand the effect of increasing the number of frames from one to two to ten.

Problem: CM20 **Area: Networking** **Code** _____

The table below is a routing table using classless interdomain routing (CIDR). Address bytes are in hexadecimal. The notation "/12" in C4.50.0.0/12 denotes a mask with 12 leading 1 bits: FF.F0.0.0.

Determine the next hop to which a packet with each of the following destination addresses will be delivered, assuming the match with the longest prefix is selected.

Show your work. Answers without work will receive no credit.

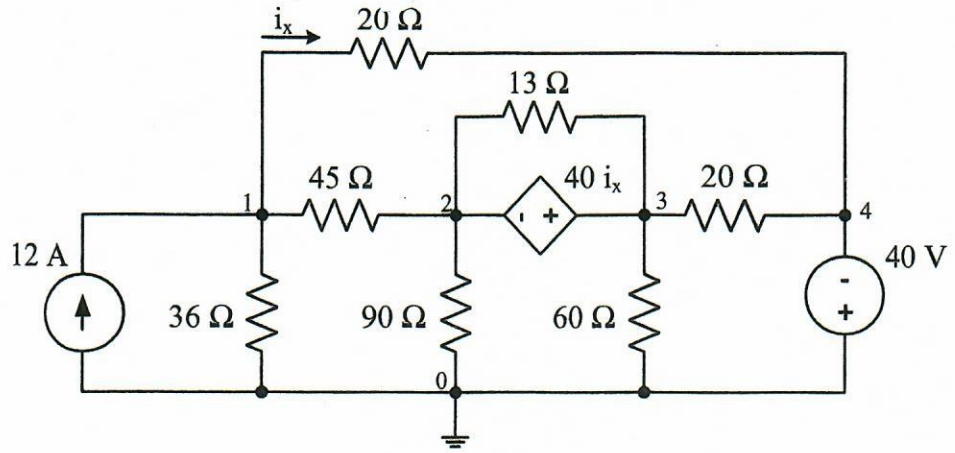
Note that the masks have been provided to you in hexadecimal format. Conversion to decimal is not necessary. Conversion of parts of the information to binary is likely to be necessary.

Net/MaskLength	NextHop
C4.5E.2.0/23	A
C4.5E.4.0/22	B
C4.5E.C0.0/19	C
C4.5E.40.0/18	D
C4.4C.0.0/14	E
C0.0.0.0/2	F
80.0.0.0/1	G

a. C4.4B.31.2E
b. C4.5E.05.09
c. C4.4D.31.2E
d. C4.5E.D1.02

M5 Area: Circuits/ Electronics Code#_____

Write a set of node-voltage equations in matrix form for the circuit below, using the space provided. (Evaluate v_1, v_2, v_3, and v_4.



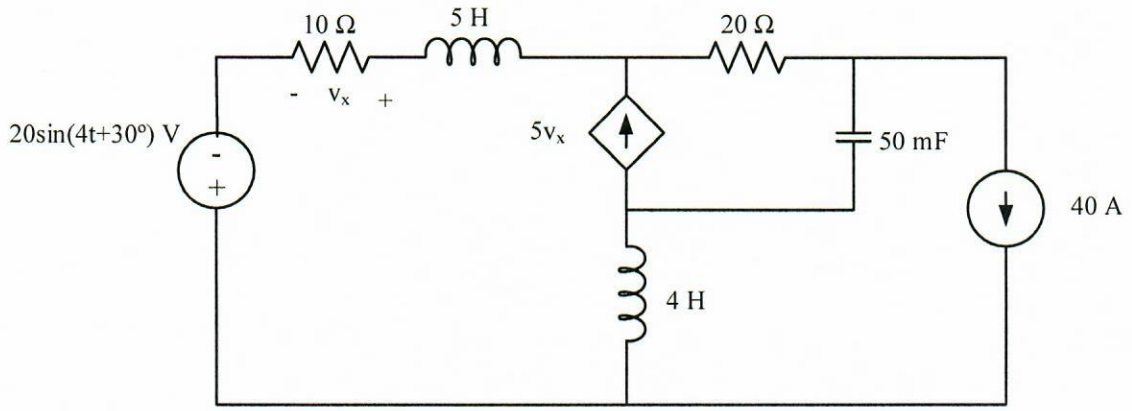
$$\begin{bmatrix} \quad \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} \quad \end{bmatrix}$$

$v_1 =$ _____ $v_3 =$ _____

$v_2 =$ _____ $v_4 =$ _____

PROBLEM M6 CIRCUITS AND ELECTRONICS AREA Code #_____

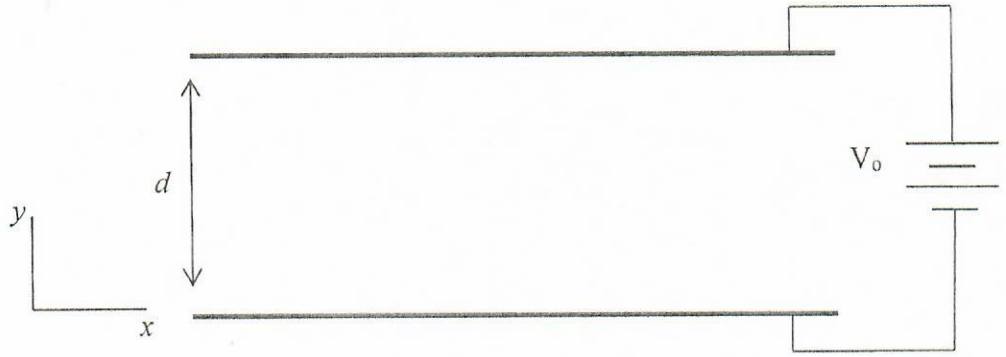
Find the steady-state voltage, $v_x(t)$, in the following circuit.



Problem: M9 Area: Waves, Devices, & Optics Code #:_____

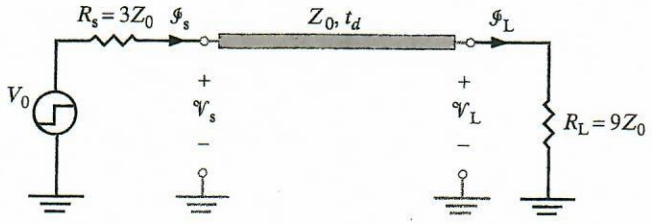
Two large conducting plates are placed a distance "*d*" apart and are located in freespace. The lower plate is held at zero potential ($\Phi = 0$), and the upper plate is held at a potential of V_o ($\Phi = V_o$). Note: edge effects can be neglected.

- Find the potential, Φ, in the region between the plates.
- Find the electric field intensity, $\overline{E}$, in the region between the plates.
- Find the electric flux density, $\overline{D}$, in the region between the plates.
- What is the surface charge density, ρ_s, on the upper and lower plates? Recall that the magnitude of the normal component of the electric flux density is equal to ρ_s.



Problem: M10 Area: Waves, Devices & Optics. Code #_____

Problem: A lossless transmission line is shown below with internal source resistance, $R_s = 3Z_0$, and load resistance, $R_L = 9Z_0$. Here Z_0 is the characteristic impedance of the transmission line. (That is $Z_0 = \sqrt{\frac{L}{C}}$ and L and C are the inductance and capacitance per unit length of the transmission line.)



(a) Sketch the bounce diagrams for the voltage and current. What are the values of the initial voltage, V_1^+ and the initial current, I_1^+ ?

(b) Plot the voltage at the load location, $V_L(t)$, as function of time, t, up to 6 times of the transit time.

(c) Plot the current at the load location, $I_L(t)$, as function of time, t, up to 6 times the transit time.

Problem #M11 **Area: Waves & Devices Code #**

Consider a silicon (Si: a Col. IV material)) abrupt-junction pn diode in which only donors are on the n-side and only acceptors are on the p-side. T = 300 K. Important physical constants are:

Boltzmann's constant:	$k = 1.38 \times 10^{-23}$ J/K = 8.62×10^{-5} eV/K		
Planck's constant:	$h = 4.14 \times 10^{-15}$ eV-s	Electronic charge:	$q = 1.60 \times 10^{-19}$ C
Carrier Mobilities	$\mu_n = 1350$ cm^2/V-s	$\mu_p = 480$ cm^2/V-s	
Bandgap Energy of Si	$E_g = 1.11$ eV		
Intrinsic Carrier Concentration	$n_i = 1.50 \times 10^{10}$ cm^{-3} at 300 K		

(a) Name the bias condition for which the following current types are dominant.

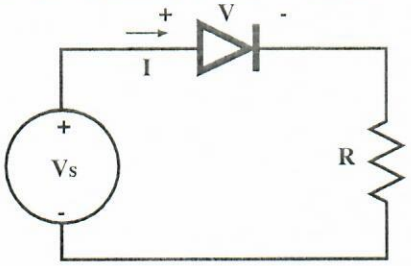
Dominant Current	Bias Condition (Reverse Bias or Forward Bias)
Diffusion Current:	_____
Drift Current:	_____

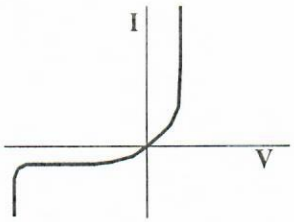
(b) If an applied voltage is present, state how the depletion region width changes relative to the equilibrium depletion width. Circle the correct choices

Forward bias:	**Increases**	**Decreases**	**Stays the same**
Reverse bias:	**Increases**	**Decreases**	**Stays the same**

(c) The contact potential is $V_o = 0.70$ V. Calculate the doping concentrations for the p and n sides if the doping concentrations on each side are equal. .

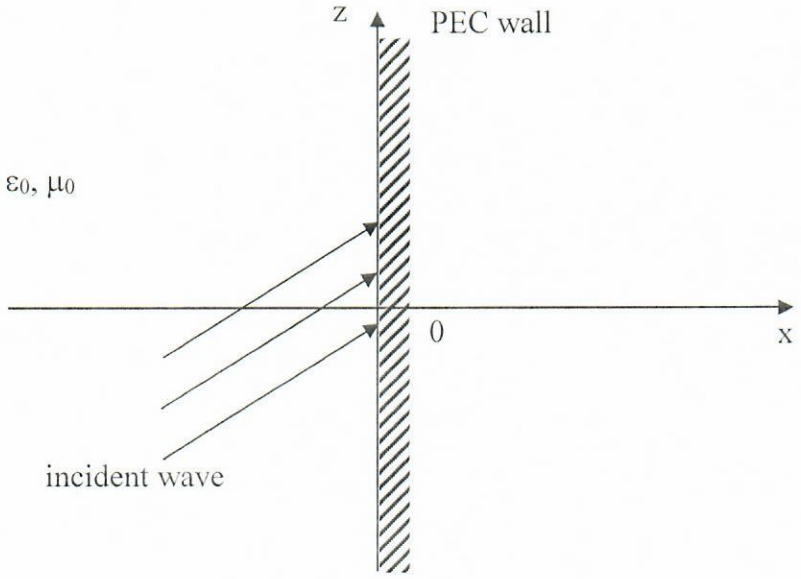
(d) For the diode circuit below, the turn-on voltage is $V_{to} = 0.70$ V, the reverse saturation current is 0.50 mA, and the breakdown voltage is -15 V. If R = 2,000 Ω and $V_S = +10 \sin(10t)$ V, calculate the operating point (V, I) for $V_S = +10$ V and $V_S = -10$ V.





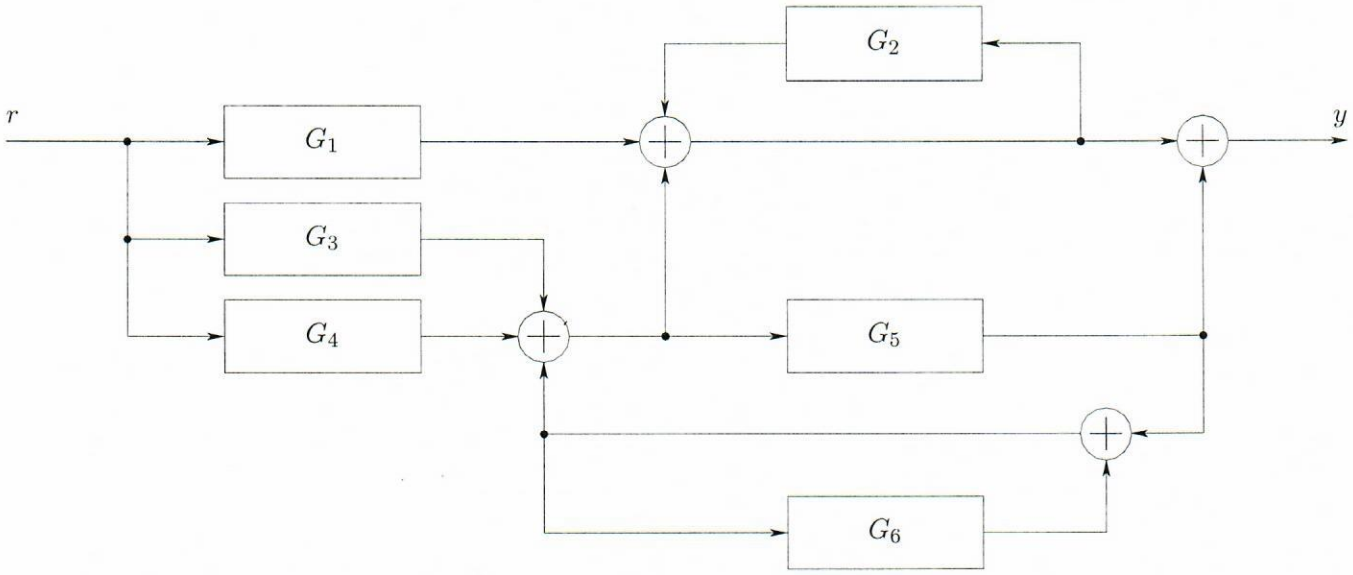
Problem: M12 Area: Waves, Devices, & Optics Code #: _____

A uniform plane wave propagating in air given by $\vec{E}_i(x,z) = \pi e^{-j120\pi x - j50\pi z}(120\hat{z} - 50\hat{x})$ (V/m) is incident on a perfect electric boundary (PEC) wall located at x = 0. Find the magnetic field of the **reflected** wave.



Prob: M13 **Area:** Control **Code #** _____

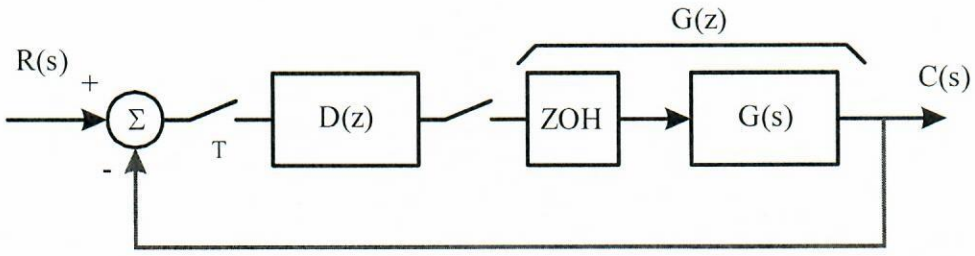
Consider the following block diagram.



Determine the transfer function. Show your work clearly.

Prob: M14 **Area:** Control **Code #**_____

Given the system below, for which three lead compensators have been designed.



$$G(z) = \frac{0.0242(z + 0.967)}{(z - 1.0)(z - 0.9048)}$$

The desired closed-loop poles are $0.677 \pm j0.246$ which correspond to 10% overshoot and a 2% settling time of 12T. The following three $D(z)$ lead compensators have been designed using root locus techniques. Rank the designs from best to worst and state your reasons for your choice. Consider such factors as good design practice, meeting design specifications when actually implemented, etc. Additional calculations are not required.

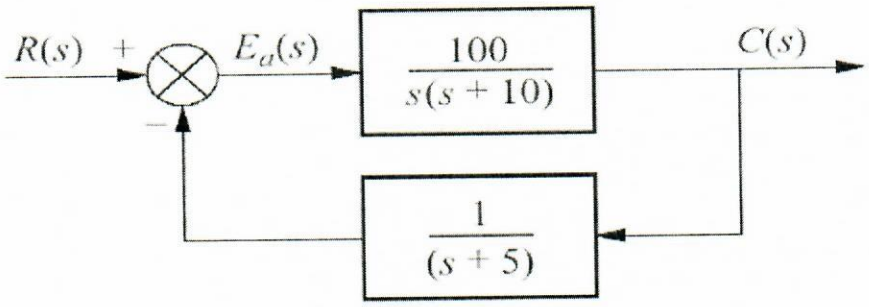
$$D_1 = 3.39\frac{(z - 0.910)}{(z - 0.443)}$$

$$D_2 = 6.42\frac{(z - 0.677)^2}{(z - 0.443)^2}$$

$$D_3 = 23.17\frac{(z - 0.554)^2}{z^2}$$

Prob: M15 **Area:** Control **Code #**_____

Consider the following system



Calculate the steady-state error for the ramp input.

A superheterodyne receiver uses an IF frequency of 455 kHz. The receiver is tuned to a transmitter having a carrier frequency of 1650 kHz.

1. Determine the frequencies of the local oscillator corresponding to low-side and high-side tuning.

2. Sketch the block diagrams of the AM transmitter and receiver, specifying all parameters if a filter is used.

In1962, AT&T first offered digital telephone transmission referred to as T1 service. With this service, each T1 frame is partitioned into 24 time-division multiplexed channels or time slots. Each time slot contains 8 bits (one speech sample), and there is one additional bit per frame for alignment. The speech signal of each channel is sampled at 8000 samples per second. The bandwidth used for transmitting the composite T1 signal is 386 kHz. Find the bandwidth efficiency (bits/s/Hz) for this signalling scheme.