**Problem: CM1** **Area: Computers and Architecture** **Code #_________**

Define and compare Harvard and van Neumann computer architectures. Give at least 3 advantages of each architecture, and corresponding applications/systems.

**Problem: CM2** **Area: Computers and Architecture** **Code #_________**

Consider the following instruction set:

| | | |
|---|---|---|
| LD A | 011xaaaa | Load A with the contents of memory location aaaa |
| LD B | 100xaaaa | Load B with the contents of memory location aaaa |
| ADD A, B | 101xxxxx | A ← A + B |
| DIV AB | 110xxxxx | A ← quotient, B← remainder |
| JNZ addr | 111xaaaa | If A is not zero, then jump to address aaaa |

a) Design a general purpose datapath which will implement these instructions. Clearly label your control and status signals and identify your components and their features.

b) Give the sequence of control signals necessary to fetch, decode, and execute each of these instructions.

**Problem: CM3** **Area: Computers and Architecture** **Code #________**

Answer the following questions.

1. Name three different hazard types of pipelined processors.

2. For the five stage MIPS pipeline processor, Indicate which of the following instructions will generate hazard, and what type of hazard?

   ADD R1, R3, R4
   ADD R5, R6, R7
   SUB R8, R1, R7
   OR R9, R7, R6

3. If there is a hazard in 2, could it be handled using forward path? If so, please indicate the forward path. If not, please explain why.

**Problem: CM4** **Area: Computers and Architecture** **Code #_________**

Below is a list of 32-bit memory address references, given as word addresses.

3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with two-word blocks and a total size of 8 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

**Problem: CM5** **Area: Integrated Circuits and Logic Design** **Code #_________**

Simplify the following Boolean expression:

$$F(A,B,C) = \overline{(A+\overline{C})}(\overline{A}+B+C)(A+\overline{B}+C)+\overline{B}$$

***You may use any appropriate method, but you must show your work for full credit.***

**Problem: CM6** **Area: Integrated Circuits and Logic Design** **Code #________**

Given the state table below with the state variables X and Y, externally applied input t, and output f. Answer the questions below.

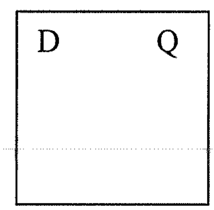
| Present Input | Present State | | Present Output | Next State | | JK Flip Flop Inputs | | SR Flip Flop Inputs | |
|---|---|---|---|---|---|---|---|---|---|
| t | X | Y | f | X* | Y* | $J_X$ | $K_X$ | $S_Y$ | $R_Y$ |
| 0 | 0 | 0 | 0 | | | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 0 | | | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | | | 1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | | | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 1 | | | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 1 | | | 1 | 0 | 0 | 1 |
| 1 | 1 | 0 | 0 | | | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | | | 1 | 0 | 0 | 1 |

a) Fill in the missing values for the state table.
b) Draw the state transition diagram based on the state table.

**Problem: CM7** **Area: Integrated Circuits and Logic Design** **Code #_________**

Make a SR flip-flop out of the D flip-flop below. Show all your work and draw the resulting circuit.

| S | R | Q | Q* | D |
|---|---|---|---|---|
| 0 | 0 | 0 | | |
| 0 | 0 | 1 | | |
| 0 | 1 | 0 | | |
| 0 | 1 | 1 | | |
| 1 | 0 | 0 | | |
| 1 | 0 | 1 | | |
| 1 | 1 | 0 | | |
| 1 | 1 | 1 | | |



**Problem: CM8** **Area: Integrated Circuits and Logic Design** **Code #_________**

Draw a cross-section of a PFET whose source and drain are connected to wires in M1. Identify each material (e.g. M1, $SiO_2$, P-Substrate, n-diffusion, p-diffusion, etc). Identify the source, gate, drain, and body. One of these terminals is (nearly) always connected to Vdd or Vss. Show the connection.

**Problem: CM9** **Area: Embedded Computer Systems** **Code #________**

The Program Status Word (PSW) register for the 8051 is organized as shown below:

(PSW.7=CY, PSW.6=AC, PSW.5=General-purpose flag, PSW.4=RS1, PSW3=RS0, PSW.2=OV, PSW.1=Not used, PSW.0=P, where CY refers to carry, AC refers to auxiliary carry, RS1 and RS0 refer to the register bank selection bits, OV refers to the overflow flag, P refers to parity)

| CY | AC | F0 | RS1 | RS0 | OV | --- | P |
|---|---|---|---|---|---|---|---|

Answer the questions for parts a and b below.

a) Determine the following values after the instruction sequence below has been executed. *Show your work for full credit.*

```
MOV PSW, #19H
MOV A, #49H
SETB C
ADDC A, #75H
```

CY: ________________

AC: ________________

OV: ________________

P: ________________

A: ________________________________

Active Register Bank (0-3):______________________

b) Write a sequence of instructions that changes the Active Register Bank to Register Bank 1 but does not change any of the other flags in the PSW.

**Problem: CM10** **Area: Embedded Computer Systems** **Code #________**

Answer the following:

a) What does the baud rate measure in serial communication?

b) Explain (a) what interrupts are and (b) what advantage they give us when designing a digital system.

c) A common function used in embedded systems programming is the DELAY subroutine. Calculate the number of machine cycles the following function consumes. Include overhead. (Note: MOV and NOP consume 1 cycle while the other instructions all consume 2. The DJNZ instruction will decrement the register and, if the register is not zero, jump to the indicated label.)

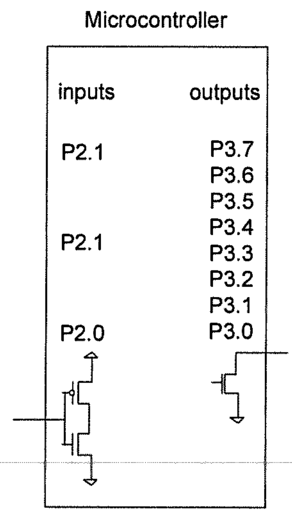
```
DELAY:MOV R3, #50
OUT:    MOV R2, #100
IN:     NOP
        DJNZ R2, IN
        DJNZ R3, OUT
        RET
```

Answer = ________________

**Problem: CM11** **Area: Embedded Computer Systems** **Code #________**

We wish to create a simple embedded system that a) reads in the value of 3 switches (i.e. the three switches are either open or closed), b) converts the result to a binary number (e.g. the switches in state open/closed/open are equivalent to a binary 010), and c) lights up one of 8 LEDs according to the buttons pushed (e.g. if a binary 010 is has, LED no. 2 is lit). Assume the microcontroller has <u>open drain</u> outputs, as indicated for P3.0 below, and with inputs that are in no way connected to power or return, also as indicated for P2.0 below.

a. Show how to hook up the microcontroller below, so that we can read the input switches and can write to the LEDs. Assume there are 8 LEDs and 3 switches.




b. Write a short segment of ASM to read the switches and write to the LEDs. You may use ASM code for the 8051 or any other microprocessor of your choosing.

**Problem: CM12** **Area: Embedded Computer Systems** **Code #________**

Answer the following two questions:

1. List at least five different criteria for choosing a microcontroller for embedded system projects. Then, clearly explain why each criterion is important.

2. What are the differences between microcontrollers and microprocessors? List at least three differences. Then, clearly explain why.

**Problem: CM13** **Area: Computational Intelligence** **Code #_________**

Explain, using equations, the motivation, design, and purposes of the backpropagation algorithm. Also include a discussion of what you consider to be its most important shortcoming (choose only one) and what can be done to mitigate that problem.

**Problem: CM14** **Area: Computational Intelligence** **Code #_________**

Give Bellman's equation and show how it can be used to convert a reinforcement learning problem into a supervised learning problem.

**Problem: CM15** **Area: Computational Intelligence** **Code #_________**

Describe in detail an unsupervised learning method of your choice.

**Problem: CM16** **Area: Computational Intelligence** **Code #________**

Give at least three advantages and disadvantages of evolutionary computation.

**Problem: CM17** **Area: Networking and Software Engineering** **Code #_________**

**Answer <u>both</u> questions below:**

1. Draw the five-layer hybrid OSI/TCP IP network model used in this course. Label each layer, and provide a one-sentence description for its main functionality.

2. Compare datagram-based to virtual circuit-based networking with respect to the following aspects:

   a. Circuit setup

   b. Addressing

   c. Routing

   d. Consequences of router failure

   e. Quality of service

**Problem: CM18** **Area: Networking and Software Engineering** **Code #_________**

**Answer both questions below:**

1. Compare the UDP and TCP protocols in terms of all four parameters below.

   a. bit overhead

   b. processing overhead

   c. reliability

   d. flexibility in supporting different types of traffic, e.g. VoIP, file transfer, telemetry

2. Compare the functions of a hub/repeater, switch, and router in computer networks. Then explain which type of node is required when connecting ATM-based and Ethernet-based networks in TCP/IP stack.

**Problem: CM19** **Area: Networking and Software Engineering** **Code #_________**

**Answer <u>all three</u> questions below.**

1. Explain the concept, operation, and capabilities of a Cyclic Redundancy Code (CRC).

2. Discuss the usage of CRCs for error detection. Give the relationship between code size and the number of bit errors that can be detected.

3. Discuss the usage of CRC for error correction Compare against its error detection applications.

**Problem: CM20** **Area: Networking and Software Engineering** **Code #________**

Eight stations, numbered 1 through 8, are contending for the use of a shared channel by using the adaptive tree walk protocol. If stations 1, 3, 5, 6, 7 suddenly become ready at once, how many bit slots are needed to resolve the contention? List the contents of each time slot.

**Problem: CM21** **Area: Security and Reliability** **Code #________**

Provide concise answers to all four questions below:

1. What is the difference between statistical randomness and unpredictability, in the context of pseudorandom number generation?

2. What are the roles of the public and private key, respectively, in asymmetric encryption?

3. What is the difference between strong and weak collision resistance, in the context of a cryptographic hash function?

4. Suppose H($m$) is a collision-resistant hash function that maps a message of arbitrary bit length into an $n$-bit hash value. Is it true that: for all messages $x$, $x'$ with $x \neq x'$, we have $H(x) \neq H(x')$?

   Justify your answer.

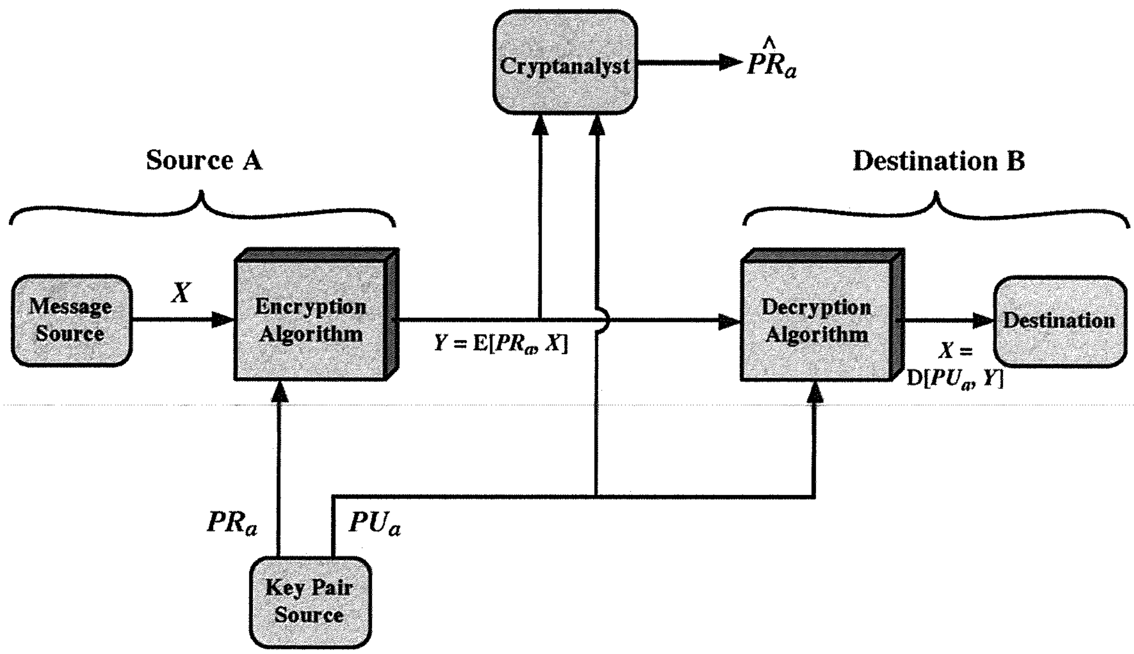
**Problem: CM22** **Area: Security and Reliability** **Code #_________**

This problem illustrates a simple application of the chosen ciphertext attack. Bob intercepts a ciphertext, $C$, intended for Alice and encrypted with Alice's public key, $e$. Bob wants to obtain the original message, $M = C^d \bmod n$. Bob chooses a random value $r$, less than $n$, and computes:

$$Z = r^e \bmod n$$
$$X = ZC \bmod n$$
$$t = r^{-1} \bmod n$$

Next, Bob gets Alice to authenticate (sign) $X$ with her private key (as in the figure below), thereby decrypting $X$. Alice returns $Y = X^d \bmod n$.

Show (mathematically) how Bob can use the information now available to him to determine $M$.



**Problem: CM23** **Area: Security and Reliability** **Code #________**

Construct the parity check matrix P for a SECDED (Single Error Correcting Double Error Detecting) Hamming code with ***k*=11** (i.e., the total number of information bits excluding parity bits is 11) and ***c*=4** (i.e., the number of parity bits is 4). Then, find Boolean equations for **check bits** and **error address bits** from the parity matrix.

**Problem: CM24** **Area: Security and Reliability** **Code #________**

Your manager in the Reliability and Quality Department asked you to verify her calculation of the reliability of a certain system. The equation that she derived is:

$$R_{system} = R_C[1-(1-R_A)(1-R_B)][1-(1-R_D)(1-R_E)] + (1-R_C)[1-(1-R_AR_D)(1-R_BR_E)]$$

Draw the system diagram based on the expression given above. Note $R_A$, $R_B$, $R_C$, $R_D$, $R_E$ are the reliabilities of components A, B, C, D and E, respectively.

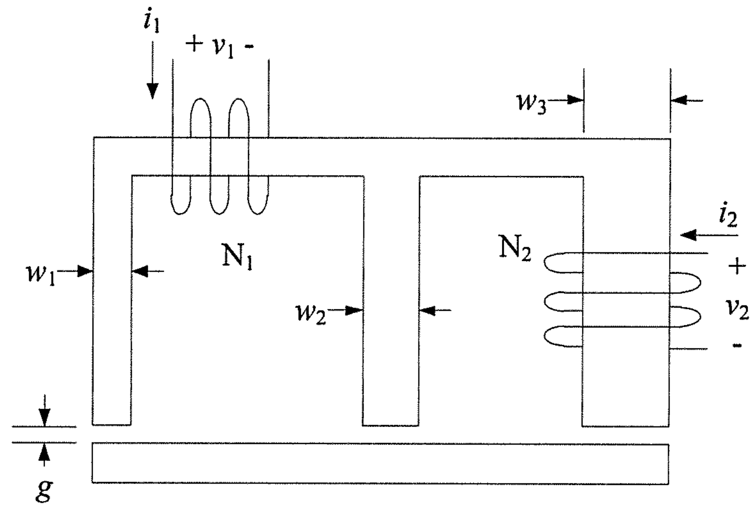
**Problem M.1** **Power/Machinery** **Code #_________**

Using a variable-frequency, constant amplitude, three-phase source; the following tests have been performed on a three-phase induction motor:

| | **Test 1** | **Test 2** |
|---|---|---|
| Frequency of three-phase source | $f_{e1} = 50$ Hz | $f_{e2} = 60$ Hz |
| Frequency of rotor signals | $f_{r1} = 1.2$ Hz | $f_{r2} = 2.4$ Hz |
| Rotor mechanical speed | $n_1$ | $n_2$ |

Find the ratio between $n_1$ and $n_2$ ($n_1/n_2 = ?$).

Consider the magnetic structure shown below. All limbs have depth into the page $d$, and the material has infinite permeability. All three gap lengths are the same, $g$. Numbers of turns, voltages, and currents are as shown.

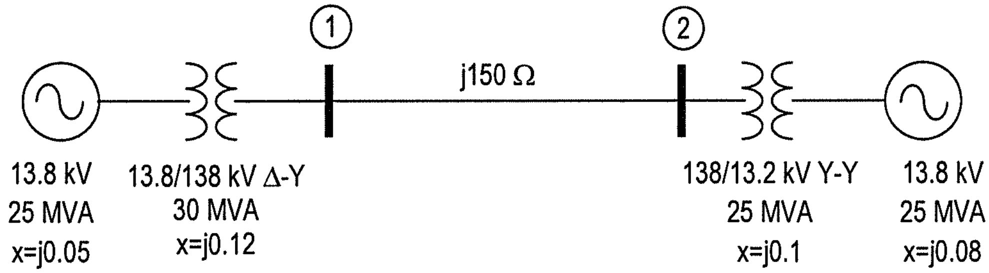



NOT TO SCALE

a. Draw the magnetic equivalent circuit. Label all polarities. Find all components symbolically.
b. Determine the flux linkages of the two coils, $\lambda_1$ and $\lambda_2$, as functions of the currents and the geometric parameters.
c. Determine the flux density $B$ in the gap that has width $w_2$ (center post) as a function of the currents and the geometric parameters.

Problem M3 Power/Machinery Code#______

Draw the per unit diagram of the system below using a 25MVA, 13.8kV base in the zone of generator 1.



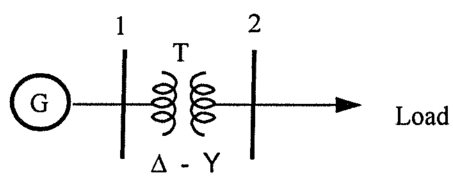
M.4 **Power/Machinery** **Code# ______**

Consider the figure below which shows the one-line diagram of a generator, a step-up transformer bank, and a load. The three-phase transformer bank T is made up of three identical single-phase transformers, each having a leakage reactance of $X_\ell = 36\ \Omega$ (on the high-voltage side) and turns ratio $a = 10$. The transformer bank delivers 80 MW at 0.8 power factor lagging to the substation HV bus whose voltage is 230 $kV_{LL}$. You may neglect the exciting current and all losses of the transformer.

(a) (15 pts) Determine the primary current magnitude

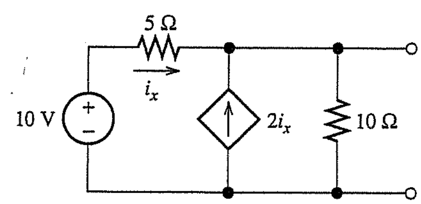
(b) (25 pts) Determine the primary voltage (line-to-line) magnitude.

(c) (10 pts) Determine the three-phase reactive power supplied by the generator.



**Prob. M5** **Area: Circuits/Electronics** **Code # ________**

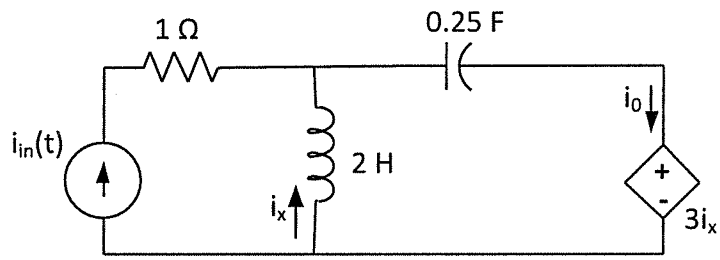
Determine the Thevenin Voltage and Thevenin Resistance for the circuit below.



For the following circuit, find:

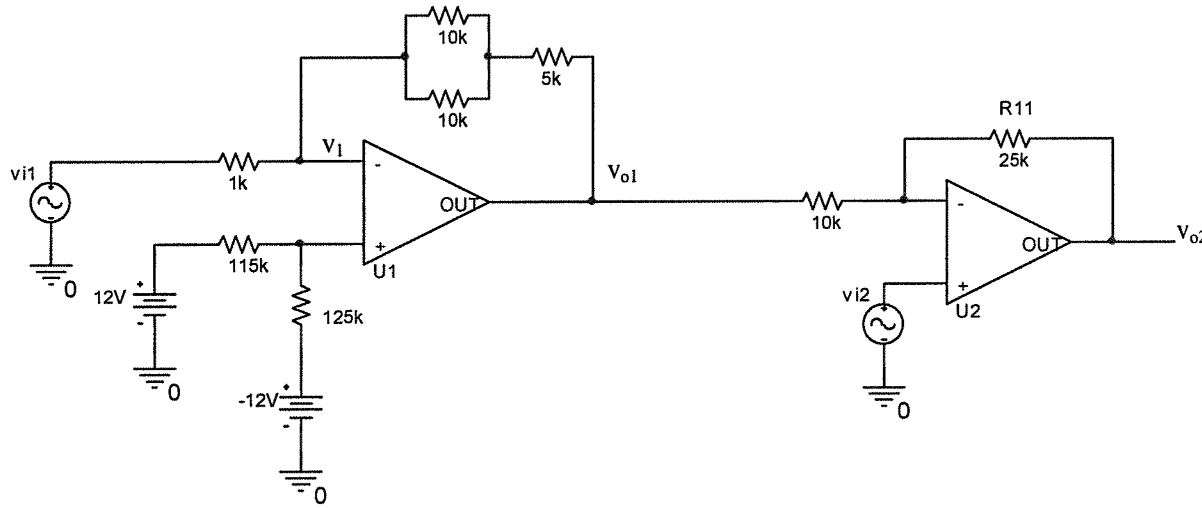
a. The transfer function $\mathbf{H}(s) = \frac{\mathbf{I_0}}{\mathbf{I_{in}}}$.

b. The steady-state output, $i_0(t)$ if $i_{in}(t) = 4e^{-2t}\cos(4t - 30°) + 4\sin(10t)$ A



**Problem M7** **Circuits/Electronics** **Code #________**

The circuit shown below is a two-stage amplifier. The operational amplifiers are assumed to be perfectly ideal, and their output voltages not to be limited by the DC power suppliers. The output voltage $v_{o2}$ can be expressed as a function of the two inputs $v_{i1}$ and $v_{i2}$ as $v_{o2} = a_0 + a_1 v_{i1} + a_2 v_{i2}$. Please determine the values of $a_0$, $a_1$, and $a_2$.



Problem: M9 Area: Waves, Devices, & Optics Code #:____________

Two infinitely long concentric metallic cylinders with the inner radius a and the outer radius b from a capacitor. The inner cylinder is maintained at potential $V_0$ and the outer cylinder is maintained at potential $V = 0$. Using the cylindrical coordinate system for electrical field components, $(E_r, E_\Phi, E_z)$ and with the aid of the Gauss's law (1) evaluate the electric field at an observation point r, where $a < r < b$. (2) relate the surface charge density on the inner cylinder $\rho_s$ with the potential value $V_0$. (3) What is the expression of the capacitance?

**Problem #M11** **Area: Waves & Devices Code #**

Consider a silicon (Si: a Col. IV material)) abrupt-junction pn diode in which only donors are on the n-side and only acceptors are on the p-side. The majority carrier concentration for the p side is $2.50 \times 10^{13}$ $cm^{-3}$ and the majority carrier concentration for the n side is $1.00 \times 10^{17}$ $cm^{-3}$. Assume T = 300 K. Important physical constants are:

| | | | |
|---|---|---|---|
| Boltzmann's constant: | $k = 1.38 \times 10^{-23}$ J/K = $8.62 \times 10^{-5}$ eV/K | | |
| Planck's constant: | $h = 4.14 \times 10^{-15}$ eV-s | Electronic charge: | $q = 1.60 \times 10^{-19}$ C |
| Carrier Mobilities | $\mu_n = 1350$ cm$^2$/V-s | $\mu_p = 480$ cm$^2$/V-s | |
| Bandgap Energy of Si | $E_g = 1.11$ eV | | |

Intrinsic Carrier Concentration $n_i = 1.50 \times 10^{10}$ $cm^{-3}$ at 300 K

**(a)** Shallow dopants for a Si host are typically ???? Circle the best single answer.

| Dopant Type | Column in the Periodic Table | | |
|---|---|---|---|
| Donor: | **Col. III** | **Col. IV** | **Col. V** |
| Acceptor: | **Col. III** | **Col. IV** | **Col. V** |

**(b)** Calculate the contact potential $V_o$.

**(c)** Calculate the diffusion coefficient for holes $D_p$ for the p side of the extrinsic Si.

**(d)** Calculate the ratio $x_{n0} / x_{p0}$ where $x_{no}$ is the equilibrium width of the depletion region on the n side and $x_{po}$ is the equilibrium width of the depletion region on the p side.

Problem: M12 Area: Waves, Devices, & Optics Code #: ____________

A uniform plane wave propagating in air given by

$$\vec{E}_i(x) = 60e^{-j40\pi x}(\hat{y} - j\hat{z}) \text{ (V/m)}$$

is normally incident on a perfectly conducting plane located at x = 0.

1) Find the frequency and the wavelength of this wave.

2) Find the corresponding magnetic field $\vec{H}_i(x)$.

3) Find the electric and magnetic field vectors of the reflected wave $\vec{E}_r(x)$ and $\vec{H}_r(x)$.

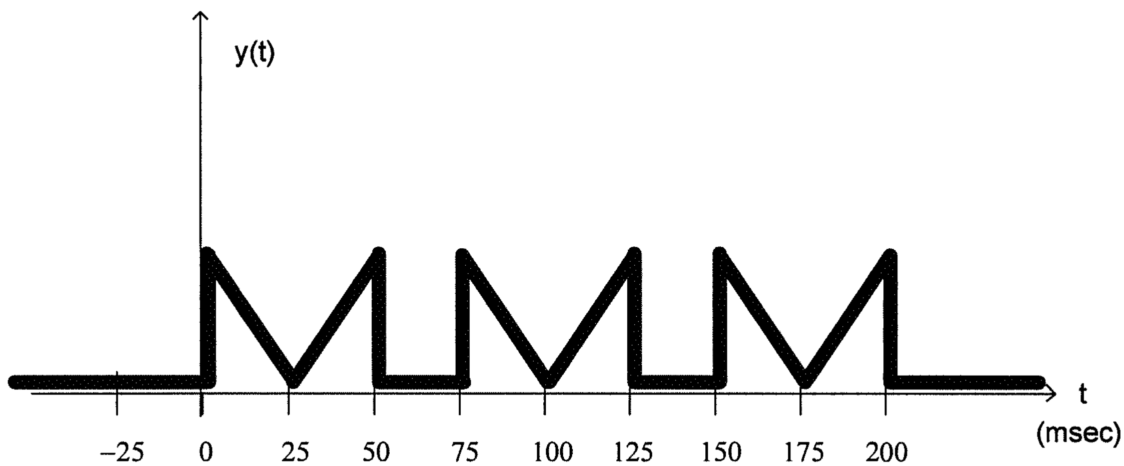
4) Find the total electric field in air $\vec{E}_{air}(x)$.

Prob. M-21 Communications / Signal Processing Code#________

A system, H, has an input of x(t) and an output of y(t). The system is linear and time-invariant, but I don't know if the system is stable or unstable. I put the following signal into the system:

$$x(t) = 0.025*\delta(t + 0.025)$$

and observe the output shown below. The signal y(t) is zero for $t < 0$ sec and $t > 200$ msec. $\delta(t)$ is a Dirac Delta function.




Answer both of the following questions, explaining your answers and showing your work for full credit. You may use the next two pages on the exam for your answer.

a) Is this system BIBO stable, unstable, or is there insufficient information to determine that?
b)
c) What is the frequency response of the system H(f), or is there insufficient information for you to calculate that?

In1962, AT&T first offered digital telephone transmission referred to as T1 service. With this service, each T1 frame is partitioned into 24 channels or time slots. Each time slot contains 8 bits (one speech sample), and there is one additional bit per frame for alignment. The frame is sampled at the Nyquist rate of 8000 samples per second, which means that one frame length is 1/(8 kHz), and the bandwidth used for transmitting the composite signal is 386 kHz. Find the bandwidth efficiency (bits/s/Hz) for this signaling scheme.