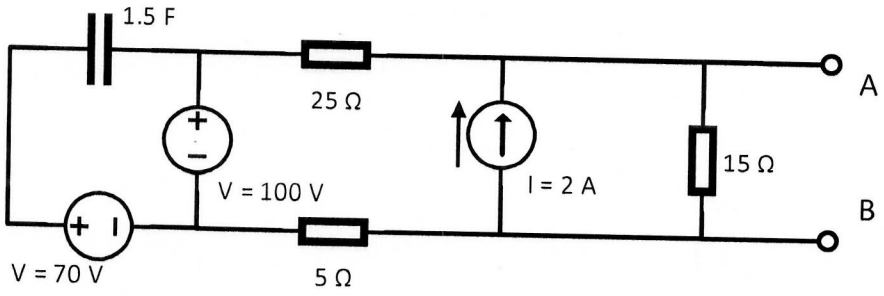
Problem : Q1, Area: Circuits/Electronics Student Code: ____

In the following steady state circuit:

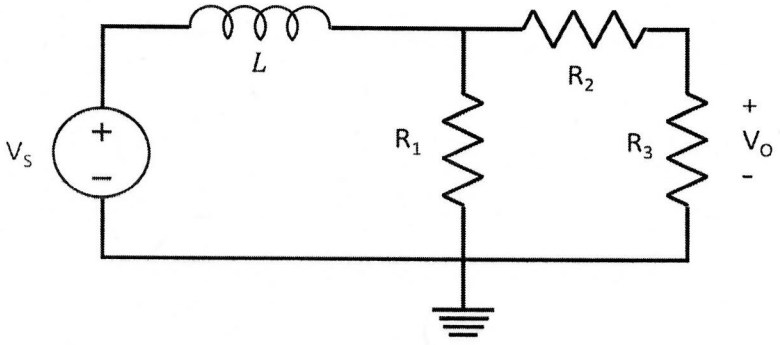
1. What is the voltage observed at AB if this port has no external load (35 points)?
2. What is the resistance observed at AB if this port has no external load (Thevenin resistance) (35 points)?
3. To receive the maximum power, what should be the resistor placed at the port AB (10 points)?
4. How much is the maximum power for part 3 (20 points)?



Problem : 2 Area: _____ Student Code: ____

For the following circuit:

Let: $R_1 = 150\Omega$, $R_2 = 50\Omega$, $R_3 = 100\Omega$, $L = 6.67mH$



a) Find the transfer function: $H(j\omega) = \frac{V_O}{V_S}$

b) What is the natural (transient) response, $v_{O_n}(t)$?

c) What is the particular response, $v_{O_p}(t)$, if $v_S(t) = 10\ cos(100t + 35°)$ V?

d) At what frequency, ω, will the angle of V_O equal zero if $v_S(t) = 10\ cos(\omega t + 35°)$ V?

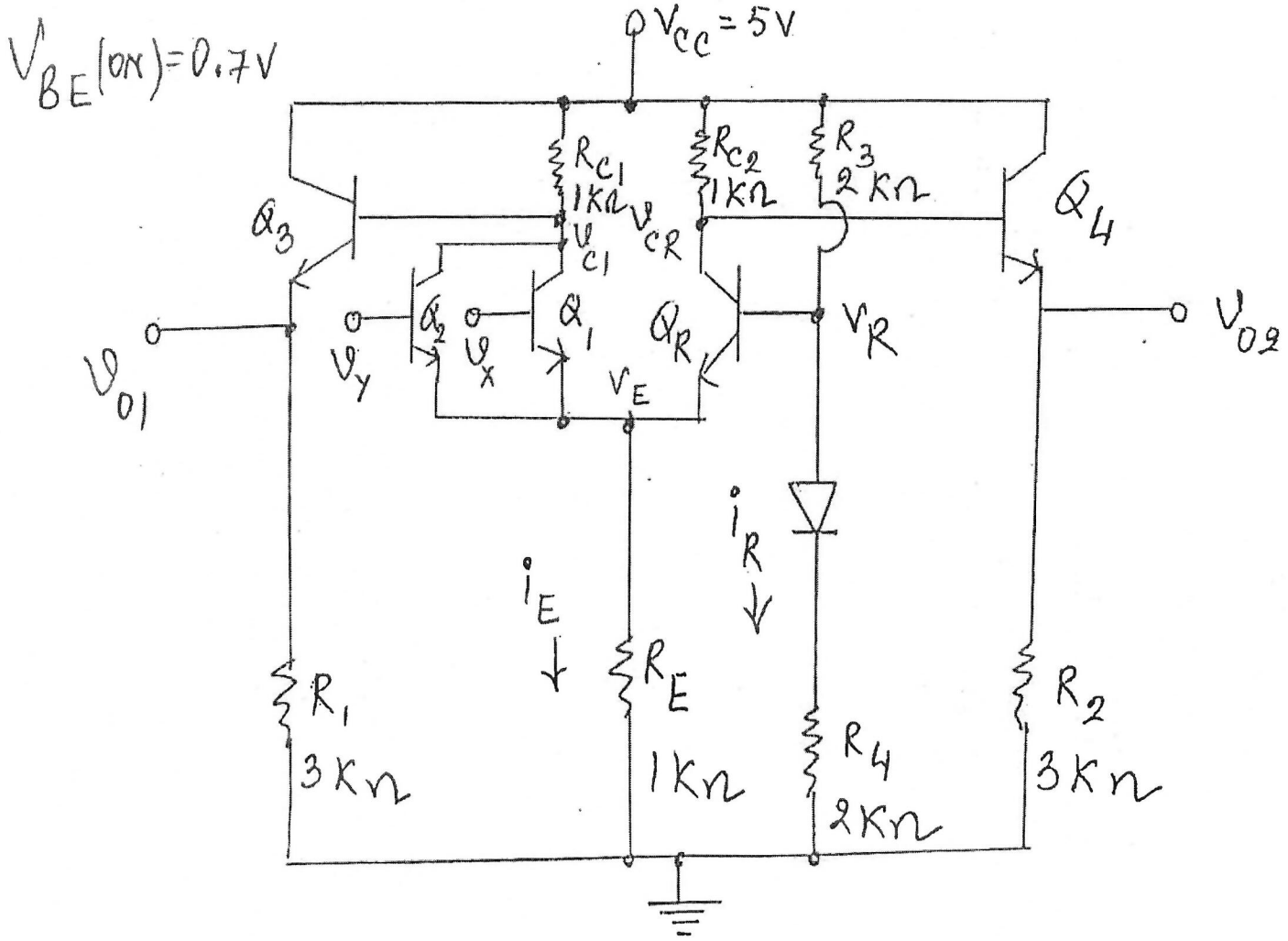
P.4

B.J. Shrestha – Ph.D. Qualifying Exam problem from Electronics (II) – Fall2021

Consider the ECL logic circuit shown below. Neglect base currents. Determine the reference voltage, V_R.

Find the logic O and logic 1 voltage values at each output v_{01} and v_{02}.

Assume that inputs v_x and v_y have the same values as the logic levels at v_{01} and v_{02}



Problem : P6 **Area: Communications / Signal Processing** **Student Code: _____**

Refer to Fig. 1 for the system with ideal Continuous-to-Discrete (C-to-D) and Discrete-to-Continuous (D-to-C) converters.

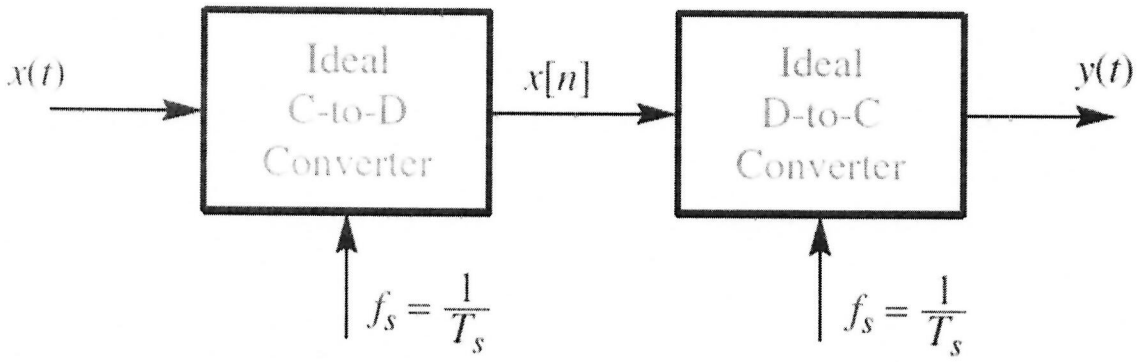


Figure 1: Ideal C-to-D and D-to-C system.

(a) Suppose that the output from the C-to-D converter is x[n] = cos(0.2πn), and the sampling rate of the C-to-D converter is f_s = 8000 samples/s. Determine a formula for the continuous-time sinusoidal input x(t) using the smallest frequency greater than 10000 Hz.

(b) Suppose the output from the C-to-D converter is x[n] = cos(0.25πn), the input signal is x(t) = cos(510πt), and the sampling rate (fs) of the C-to-D converter is less than 130 samples/s. Determine the largest possible sampling rate satisfying these three conditions.

Problem : P7 **Area: Communications / Signal Processing** **Student Code: _____**

Let a be a random variable which is uniformly distributed on the interval $[0,2]$. Define two random variables X and Y as

$$X \triangleq \min\{a, 2-a\},$$
$$Y \triangleq \max\{a, 2-a\},$$

and let $Z \triangleq \frac{Y}{X}$.

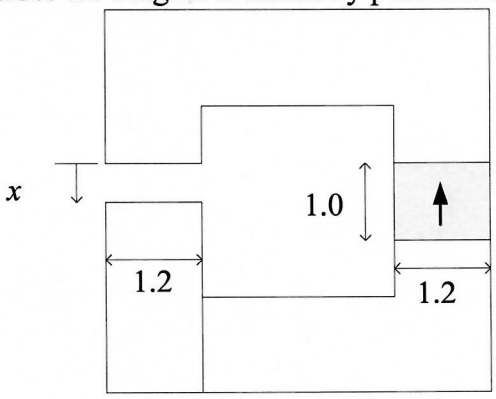
(1) Please derive the probability density function of X.

(2) Please derive the probability density function of Z.

(3) Please calculate the expectation of $\frac{X}{Y}$.

Problem: P13 **Area: Power/Machinery** **Student Code:____**

The structure below contains a permanent magnet (gray) that may be modeled with an equivalent coercivity of -850 kA/m and a recoil permeability of $1.06\mu_0$. Dimensions are given in centimeters. Depth into the page is 3.0 cm. The dimension marked "x" is free to change (notice the seam in the structure). Everything besides the magnet is infinitely permeable.



Useful equations:

$$\mu_0 = 4\pi \times 10^{-7}\, H/m \qquad \mathcal{R} = \frac{\ell}{\mu A}$$

$$W'_{fld} = \int_0^i \lambda(\hat{i}, x)\, d\hat{i} \qquad (Ni)_{eq} = -H'_c d$$

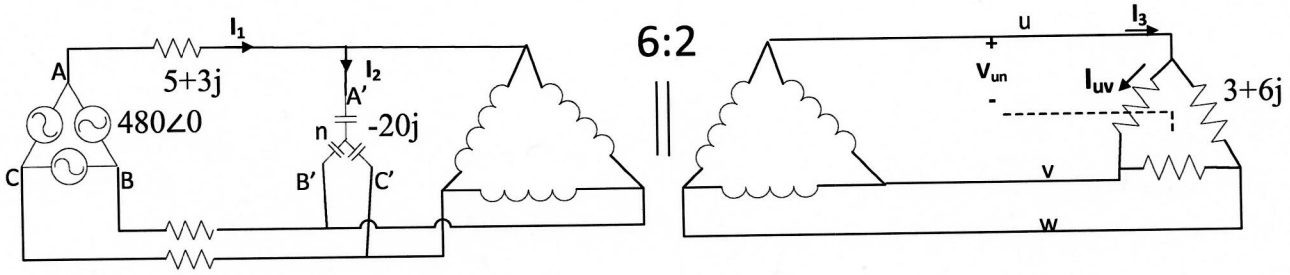
$$f_{fld} = \frac{\partial W'_{fld}}{\partial x}$$

a. Draw the magnetic equivalent circuit with the permanent magnet converted to a Thevenin equivalent (mmf source plus reluctance). Label elements both symbolically and numerically.
b. Solve the MEC to find the flux linkage in the equivalent winding.
c. Find the co-energy as a function of the equivalent current and x. You may have fictitious quantities at this point.
d. Find an expression for the force with only physical quantities included, meaning no equivalent turns or current.

Problem : 14 **Area:** _____ **Student Code:** ____

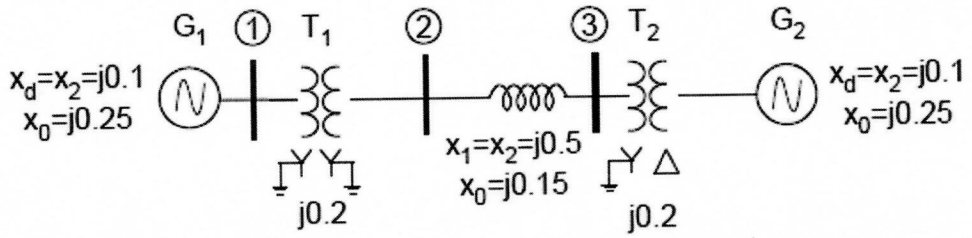
In the following circuit, find the following (both amplitude and angle):

a) I_1, I_2, and I_3 (40 points).
b) I_{uv} (output resistor's current) (20 points).
c) Phase voltage of the load equal to V_{un} (20 points).
d) 3-phase complex power of the source (20 points)



Problem: 16 **Area: Power** **Student Code:_____**

In the system shown below, a solid single line-ground fault occurs on bus 3. Both generators are solidly grounded.



The prefault voltages are 1.0 per unit. What are the positive, negative and zero sequence fault currents in line 2-3 during the fault?

Problem : 17 **Area: Waves & Devices** **Student Code:____**

Air-perfect conductor interface. A uniform plane electromagnetic wave traveling in the air with its electric field given by $\bar{E}_i(x,t) = \hat{y}15\cos(44\times10^9 t - \beta x)$ V/m is normally incident on a perfect conductor boundary located at x = 0. (a) Find the propagation constant β. (b) Find the corresponding magnetic field $\bar{H}_i(x,t)$. (c) Find the electric and magnetic fields $\bar{E}_r(x,t)$ and $\bar{H}_r(x,t)$ of the reflected wave. (d) Find the nearest two positions in the air away from the boundary where the total electric field is always zero.

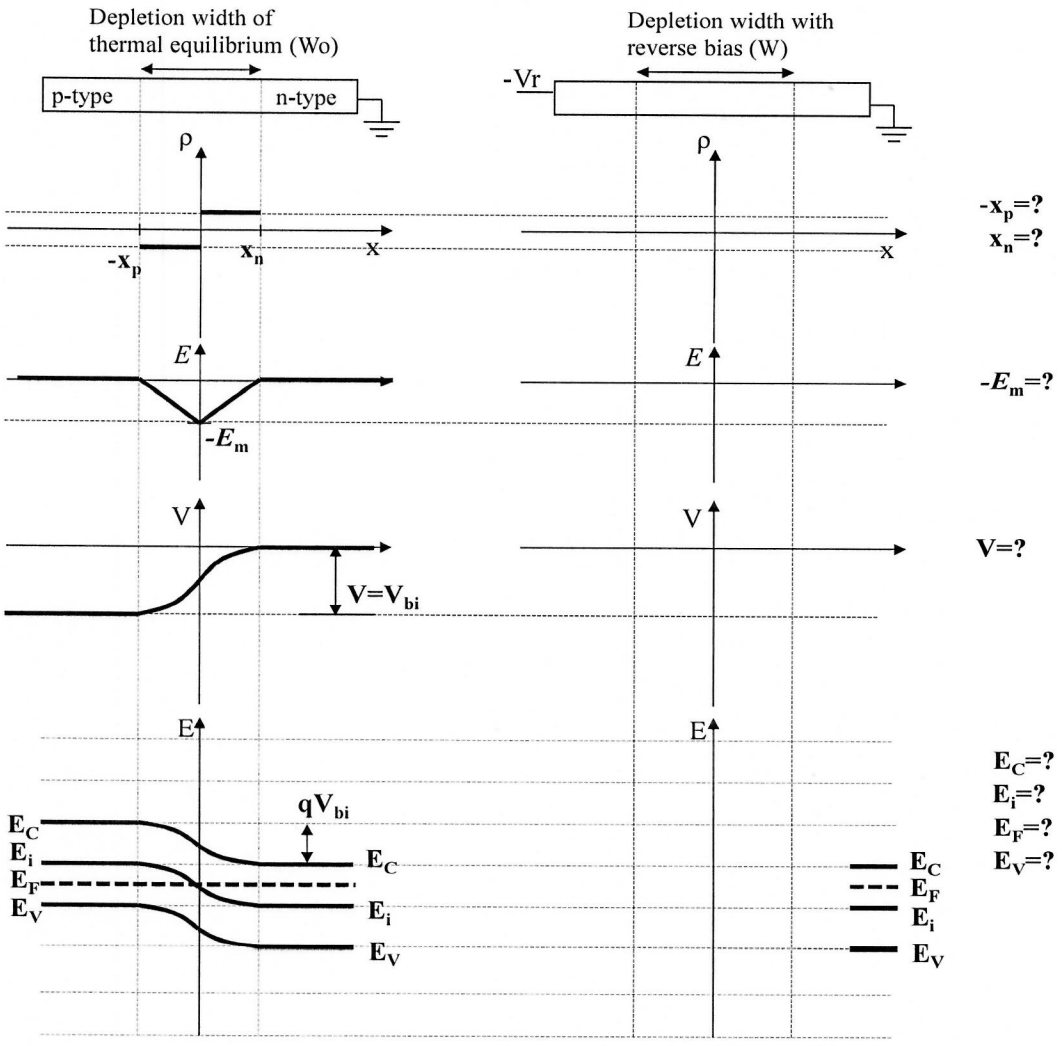
Problem : 19 **Area: Waves & Devices** **Student Code:____**

1. [30%] An abrupt silicon p-n junction diode has a net acceptor concentration $10^{17}cm^{-3}$ in the p-side and a net donor concentration $10^{17}cm^{-3}$ in the n-side, respectively. Calculate the potential difference (i.e. contact potential or built-in potential) across the depletion region (or space charge region) at thermal equilibrium in room temperature (300K).

Constants*	Equations*
▪ Elementary charge = 1.6×10^{-19} [C] ▪ kT = 0.0259 [eV], kT/q = 0.0259 [V] (at 300 K) ▪ Intrinsic concentration = 9.65×10^{9} [cm^{-3}] (for silicon at 300 K)	▪ $n_o p_o = n_i^2$ ▪ $n_o = n_i \exp[(E_F - E_i) / kT]$ or $(E_F - E_i) = kT \ln(n_o/n_i)$ ▪ $p_o = n_i \exp[(E_i - E_F) / kT]$ or $(E_i - E_F) = kT \ln(p_o/n_i)$ ▪ $\sigma = q(n\mu_n + p\mu_p)$

* Definitions of parameters are not given. It is expected that the examinees interpret the meaning.

2. [35%] Complete the diagrams and mark all question-marked items of the reverse-biased symmetric p-n junction (i.e. Show the expected difference when a reverse bias is applied). Assume the n-side is electrically grounded. The dashed lines serve only as "reference lines" to indicate the value of each item in the equilibrium condition.



Problem: 21 **Area**: Computational Intelligence **Code #**_____

(a) What is Computational Intelligence (CI)?

(b) Describe the different between the traditional Artificial Intelligence (AI) and the modern CI. Give an example of an application where AI is the more appropriate paradigm. Give an example of an application where CI is the more appropriate paradigm. Justify your application selections for AI and CI.

Problem: 22 **Area**: Computational Intelligence **Code #**_____

Answer the questions for parts a, b, and c below.

(a) What is the difference between supervised, unsupervised learning and reinforcement learning?

(b) Describe one application where CI is used with each of the following: (a) supervised learning, (b) unsupervised learning, and (c) reinforcement learning.

(c) Multilayer perceptrons (MLPs) and Radial-basis function (RBF) networks are examples of feedforward neural networks. They are both universal approximators. However, these two networks differ from each other in several important ways. Describe **three** differences.

Problem: 24 **Area**: Computational Intelligence **Code #**_____

Answer the questions for parts a and b below.

(a) Describe the different types of hardware evolution. Provide diagrams where possible.

(b) Define the following terms:

(i) Embryonics

(ii) Deep Learning

Problem: 25 Area:_____ **Student Code:**____

Suppose you are given a simple memory hierarchy with a **direct-mapped** cache memory which can store **8 one-word data blocks** and a **word-addressable** main memory which can store **16 data words**. For a word address sequence of 0000, 1000, 0000, 1000, 1100, 0100 and 1100 in binary, **complete the following table** by showing: tag, index, hit/miss and cache contest after each access. Then, **calculate its hit ratio**.

Add	Tag	Index	Hit/ Miss	Cache content after access							
				000	001	010	011	100	101	110	111
0000											
1000											
0000											
1000											
1100											
0100											
1100											

Hit ratio =_____

Problem: 26 **Area**: Computer Architecture and Embedded Systems **Code #**_____

Describe the difference between a Von Neumann architecture and a Harvard architecture. Which architecture is more advantageous for systems that use a microcontroller and for systems that use a general-purpose microprocessor? Explain your answer.

Problem :___2x____ 27 **Area:**____ Computer Architecture and Embedded Systems ____ **Student Code:**____

Note: Read the question carefully and make sure your answer is clear and readable.

a) Name and elaborate on at least three major shortcomings of a **scalar pipeline architecture** in its evolution to a **superscalar design**:

i.

ii.

iii.

Problem : 28 Area: _____ Student Code: ____

a) (25%) What are some of the most important differences between a microprocessor and a microcontroller?

b) (25%) What is the function of a Status Word register in the 8051 (or similar microcontroller)? Give example of information stored in such a register.

c) (50%) Write a code that reads the input value "n" stored in register R7 and displays first "n" numbers from Fibonacci sequence (stored in #TABLE). The code should fetch each Fibonacci number and display it on port 2 (P2). For example, if R7 = 5, then write to P2 sequence of "0", "1", "1", "2", "3" numbers. Make sure to insert a delay after displaying each number – by using an already existing subroutine at address #DELAY. The look-up table containing the series is already created in the first two assembler instructions provided below. (You can assume any general assembly language – e.g. 8051– please indicate which one is used).

```
ORG 300H
TABLE: 0, 1, 1, 2, 3, 5, 8, 13, 21, 34, 55, 89, 144, 233
PRINT_FIBONACCI:
```

Problem: CM29 **Area: Integrated Circuits and Logic Design** **Code #**_____

Answer the questions for parts **a** and **b** below.

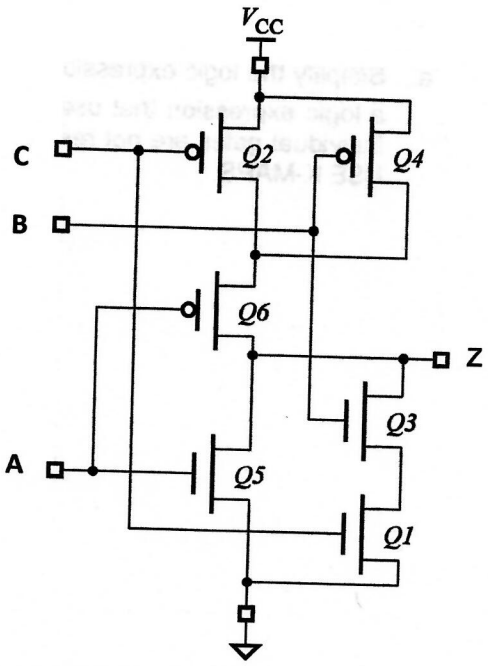
a. Simplify the logic expression $F(a,b,c) = (\bar{a}+\bar{b})(\bar{c}+\bar{b})(a+\bar{b}+c)$ using algebraic manipulation to obtain a logic expression that uses as few gates as possible (exclude inverters from the total gate count). Individual gates are not restricted on the number of inputs. *Show your work for full credit.* DO NOT USE K-MAPS.

b. Construct the truth table for $F(a,b,c) = (\bar{a}+\bar{b})(\bar{c}+\bar{b})(a+\bar{b}+c)$.

Problem: CM30 **Area: Integrated Circuits and Logic Design** **Code #**_____

Answer the questions for parts **a** and **b** below.

a. For the CMOS circuit shown to the right, indicate whether each transistor is ON or OFF and the function output Z (H or L).



A	B	C	Q1	Q2	Q3	Q4	Q5	Q6	Z
L	L	L							
L	L	H							
L	H	L							
L	H	H							
H	L	L							
H	L	H							
H	H	L							
H	H	H							

b. Determine the logic function for Z from the CMOS logic circuit in part **a**.

Problem: CM31 **Area: Integrated Circuits and Logic Design** **Code #_____**

Design a 2-bit down counter 32103210... using JK flip-flops, including drawing the counter circuit. Show your design steps for full credit.

Problem: CM32 **Area: Integrated Circuits and Logic Design** **Code #_____**

Draw a circuit to implement the function $f(w,x,y,z) = \sum m\,(0,1,2,4,5,7,8,9,11,14,15)$ using a 4:1 MUX and other logic gates as needed. You may use the truth table to help if needed.

w	x	y	z	f
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Problem: P33 **Area: Networking, Security and Dependability** **Student Code: ____**

A network data frame consists of two words of 16 bits each. Assume the probability of a bit error is 10^{-3} and that bit errors are independent. Answer all three parts below. Show your work.

a. What is the frame error probability, i.e., the probability that the received frame contains at least one error?

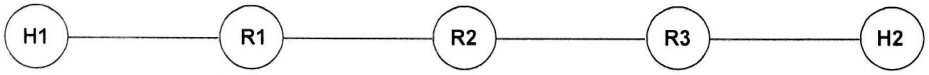
b. Consider a modified frame structure, where a single parity bit is added to each data word. With this modified frame structure, what is the frame error probability?

c. Consider the original frame structure (not part b). Now assume that a CRC-16 error detection code is added to the transmitted frame, with a generator polynomial of $(x^{16} + x^{12} + x^5 + 1)$. Answer both questions below for this case.
   a. How many bits is the transmitted frame?
   b. What is the frame error probability?

Problem: P34 **Area: Networking, Security and Dependability** **Student Code: ____**

Answer both questions below. Show your work.

a. Consider a network of two hosts connected by three routers, as depicted below. Each link has a propagation delay of 50 ms. The H1-R1 and R2-R3 links, respectively, have a data rate of 10 Mbps. Each of the other two links has a date rate of 12 Mbps. The routing and/or queuing delays at each node are negligible.



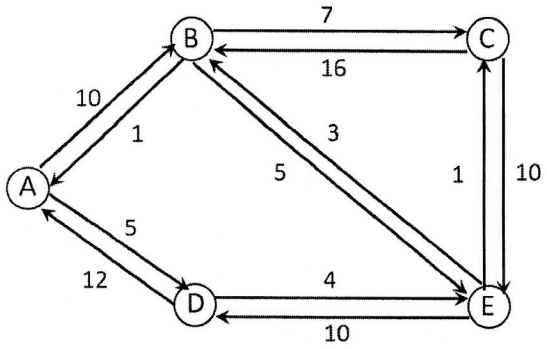
Consider a 1 MB message sent from H1 to H2 using virtual circuit packet switching with 10 KB packets. Each packet has a 50 B header, which is a negligible fraction of the overall packet. Calculate the end-to-end delay, including teardown.

b. An organization has a class C network with IP address 223.0.5.0 and wants to form respective subnets for three departments. These departments are D1, D2, and D3; which require 99, 63, and 35 hosts, respectively.

Give a possible arrangement of subnet masks to make this possible. Your final answer should include one subnet mask for each of the three departments, assigned such that any potential host address can be unambiguously associated with only a single department. Use the fewest possible number of table entries. Show your work.

Problem: P35 **Area: Networking, Security and Dependability** **Student Code: ____**

Answer questions a and b for the network shown below.



a. Use Djikstra's algorithm to determine the shortest paths from node A to each of the other nodes.

b. Assume that the A to B and B to A links fail simultaneously. The protocol does not need to repeat computations that are not affected by the failures. Show the operation of the algorithm to update the routing table.

Problem: P36 **Area: Networking, Security and Dependability** **Student Code: ____**

Each of the figures below shows encryption with three applications of DES, in the cipher block chaining (CBC) mode. The top figure is the one-loop version, and the bottom figure the three-loop version. Assume that a single stage of encryption or decryption with DES takes *T* time units, and the time for XOR operation is negligible. With this assumption, the one-loop cipher will take 3*T* to generate the ciphertext for a single block of plaintext.

a. Compare the efficiency of the two methods, in terms of the amount of time each takes to produce the ciphertext for a three-block message.

b. Is one method more secure than the other? Why or why not?