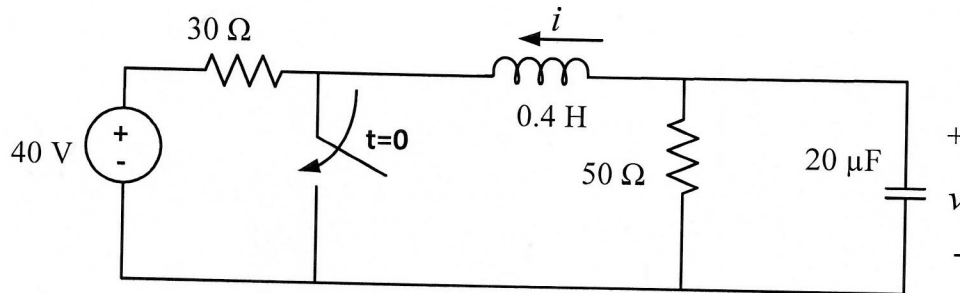
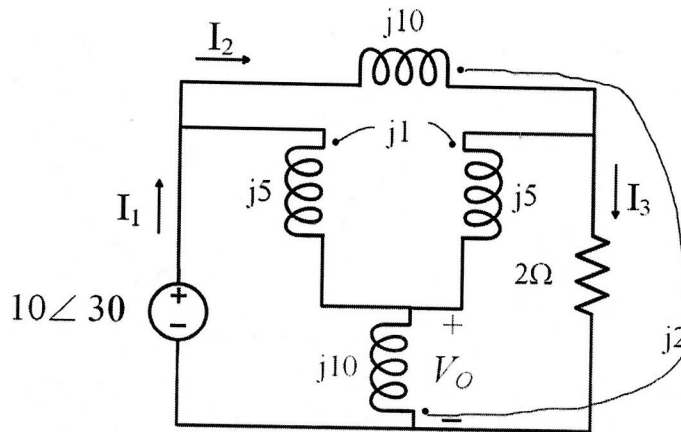


1. For the following circuit, determine the
  - a. Initial conditions of the capacitor voltage and inductor current at  $t=0$ ;
  - b. The transient response of the capacitor voltage  $v(t)$   $t>0$ ;
  - c. Is the circuit overdamped, underdamped or critically damped?
  - d. The complete response of the capacitor voltage  $v(t)$   $t>0$ .



For the following circuit, answer Parts a) and b):



- a) (20 pt) Write the set of Mesh-Current equations and fill in the matrix provided.
- b) (5 pt) Solve for  $V_o$ .

$$\begin{bmatrix} \underline{\hspace{2cm}} & \underline{\hspace{2cm}} & \underline{\hspace{2cm}} \\ \underline{\hspace{2cm}} & \underline{\hspace{2cm}} & \underline{\hspace{2cm}} \\ \underline{\hspace{2cm}} & \underline{\hspace{2cm}} & \underline{\hspace{2cm}} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} \underline{\hspace{2cm}} \\ \underline{\hspace{2cm}} \\ \underline{\hspace{2cm}} \end{bmatrix}$$

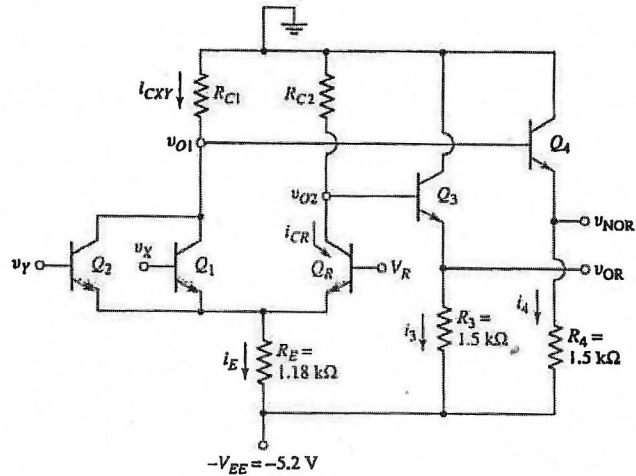
$V_o =$

Problem : 4

Area Electronics

Student Code \_\_\_\_\_

Consider the following Emitter Controlled Logic (ECL) circuit. Determine  $R_{C1}$  and  $R_{C2}$  such that when  $Q_1$ ,  $Q_2$ , and then  $Q_R$  are conducting, the B-C voltages are zero. Assume  $V_{BE(on)} = 0.7 \text{ V}$



Refer to Fig. 1 for the system with ideal Continuous-to-Discrete (C-to-D) and Discrete-to-Continuous (D-to-C) converters.

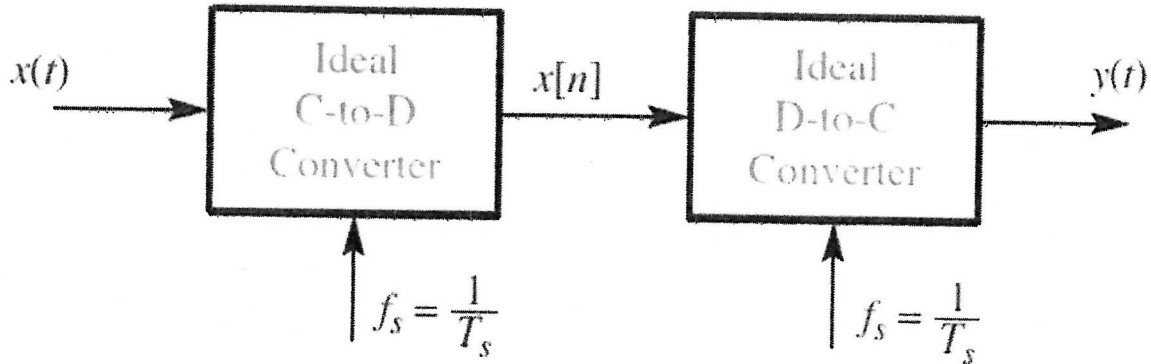


Figure 1: Ideal C-to-D and D-to-C system.

- (a) Suppose that the output from the C-to-D converter is  $x[n] = \cos(0.2\pi n)$ , and the sampling rate of the C-to-D converter is  $f_s = 8000$  samples/s. Determine a formula for the continuous-time sinusoidal input  $x(t)$  using the smallest frequency greater than 10000 Hz.
- (b) Suppose the output from the C-to-D converter is  $x[n] = \cos(0.25\pi n)$ , the input signal is  $x(t) = \cos(510\pi t)$ , and the sampling rate ( $f_s$ ) of the C-to-D converter is less than 130 samples/s. Determine the largest possible sampling rate satisfying these three conditions.

**Problem : P7**

**Area: Communications / Signal Processing**

**Student Code: \_\_\_\_\_**

Let  $a$  be a random variable which is uniformly distributed on the interval  $[0,2]$ . Define two random variables  $X$  and  $Y$  as

$$X \triangleq \min \{a, 2 - a\},$$

$$Y \triangleq \max \{a, 2 - a\},$$

and let  $Z \triangleq \frac{Y}{X}$ .

- (1) Please derive the probability density function of  $X$ .
- (2) Please derive the probability density function of  $Z$ .
- (3) Please calculate the expectation of  $\frac{X}{Y}$ .

A three-phase 2-pole round-rotor synchronous generator has a synchronous reactance of  $3.3 \Omega$  and is connected to a 4160 V three-phase bus. Useful equations:

$$P_a = \frac{V_a E_a}{X_s} \sin \delta$$

$$Q_a = \frac{V_a E_a}{X_s} \cos \delta - \frac{V_a^2}{X_s}$$

- a. For an output three-phase active power of 2.1 MW, determine the *minimum generated voltage*, corresponding torque angle, and corresponding line current magnitude.
- b. For an output three-phase active power of 2.1 MW, determine the *minimum line current*, corresponding generated voltage, and corresponding torque angle.

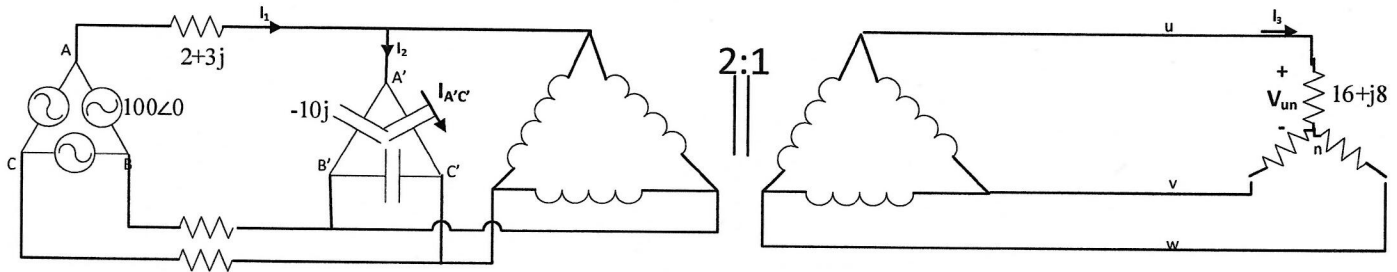
**Problem: P14**

**Area: Power**

**Student Code: \_\_\_\_\_**

In the following circuit, find the following:

- a)  $I_1, I_2,$  and  $I_3$  (60 points).
- b)  $I_{A'C'}$  (Capacitor current) (10 points).
- c) Phase voltage of the load ( $16+8j$ ) equal to  $V_{un}$  (10 points).
- d) 3-phase complex power of the source (20 points)

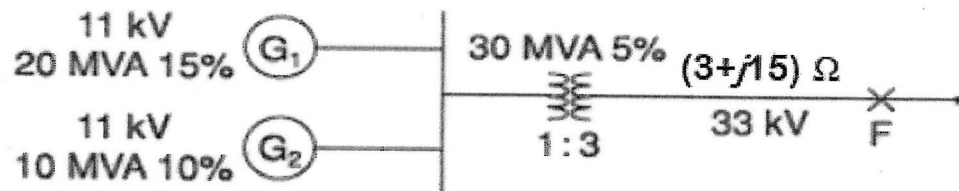


**Problem: 16**

**Area: Power**

**Student Code: \_\_\_\_\_**

In the system shown below, a three-phase short circuit occurs at point F. Assume that pre-fault currents are zero and that the generators are operating at rated voltage. Choose base MVA as 30 MVA and the base line voltage at the HV-side of the transformer to be 33kV. Determine the fault current in per unit.





**Problem: P21**

**Area:** Computational Intelligence

**Code #** \_\_\_\_\_

You have been provided a dataset with 64,000 grayscale images with handwriting examples. The images contain the alphabetic characters a-k, the Greek characters  $\Omega$ ,  $\phi$ ,  $\Sigma$ . The alphabetic characters are darker than the surrounding background. The characters are organized into character strings of uniform rows from top to bottom of each image. Some images have greater contrast between the characters and the surrounding background, and some images are blurred due to the image collection process.

You are asked to develop computational intelligence techniques to detect and count the number of occurrences of each character in the dataset.

Answer the following questions.

(a) Describe the process that you would use to process the image data to detect the individual characters and the classification process.

(b) Describe the considerations for selecting and applying a computational intelligence technique(s) for the character detection and character classification problem.

**Problem: P22**

**Area:** Computational Intelligence

**Code #** \_\_\_\_\_

Describe the different between evolutionary computing and machine learning. Give an example of an application where evolutionary computing is the more appropriate paradigm. Give an example of an application where machine learning is the more appropriate paradigm. Justify your application selections for evolutionary computing and machine learning.

**Problem: P23**

**Area: Computational Intelligence**

**Code # \_\_\_\_\_**

Answer the questions for parts a, b, and c below.

- (a) Give three examples of computational intelligence techniques that use supervised learning. Explain how supervised learning is used with each computational intelligence technique.
- (b) Give three examples of computational intelligence techniques that use unsupervised learning. Explain how unsupervised learning is used with each computational intelligence technique.
- (c) Given an example of a computational intelligence technique that can learn using incomplete or missing data.

**Problem: P24**

**Area: Computational Intelligence**

**Code #\_\_\_\_\_**

Answer the follow questions.

- a) When applying CI techniques to a given dataset, the dataset is broken up into training, cross-validation, and test sets. Describe three data normalization approaches that can be applied to the dataset. Give two considerations for determining which normalization approach is most appropriate for the application of the CI technique.

- b) Describe three metrics that can be used to assess the accuracy/correctness of the CI technique based on the test set results. Describe how you would select which metric is most appropriate for your dataset and test set results.

Problem: P29

Area: Integrated Circuits and Logic Design

Code # \_\_\_\_\_

Answer the questions for parts **a** and **b** below.

- a. Simplify the logic expression  $G(a,b,c) = (ab + \bar{c})(\bar{b}c + \bar{a})(\bar{a} + c)$  using any appropriate method to obtain the minimal sum-of-products (SOP) expression. Individual gates are not restricted on the number of inputs. *Show your work for full credit.*
- b. Draw the logic network (digital circuit) for the minimal SOP from part a. The logic gates are not restricted with the number of inputs.

Problem: P30

Area: Integrated Circuits and Logic Design

Code # \_\_\_\_\_

Answer the following questions.

a) Convert to binary:

9CD (hex) =

b) Convert to binary:

179.3125 (decimal) =

c) Convert to octal:

1110110110010.1110110 (binary) =

**Problem: P30**

**Area: Integrated Circuits and Logic Design**

**Code # \_\_\_\_\_**

d) Convert -61 to 8 bit 2's complement representation.

e) Perform the 2's complement multiplication 11001 x 11010

f) Perform the following two's complement addition operations. Give your answer as an 8-bit two's complement number. State whether overflow occurs.

1 1 1 0 1 1 1 0  
+ 1 0 1 1 1 0 1 1

0 1 0 1 0 1 1 0  
+ 0 0 1 1 0 0 1 1

**Problem: P31**

**Area: Integrated Circuits and Logic Design**

**Code # \_\_\_\_\_**

Design a 2-bit up counter with the state sequence specified as 01230123... using SR flip-flops, including drawing the counter circuit. Show your design steps for full credit.



Problem: P32

Area: Integrated Circuits and Logic Design

Code # \_\_\_\_\_

Draw a circuit to implement the function  $g(w, x, y, z) = \sum m(1,3,4,5,8,9,10,11,13,15)$  using two 3-to-8 decoders with active low outputs and active high enables. You may use other logic gates as needed for the implementation of the decoder circuit.

w	x	Y	z	g
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	1	0	1	
0	1	1	0	
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	



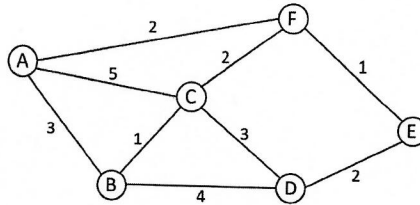
Problem: P34

Area: Networking, Security, and Dependability

Student Code: \_\_\_\_\_

This problem has two parts. For full credit, you must answer both parts correctly.

Answer the following questions for the network shown below:



- a. Suppose each node runs the Distance Vector Routing Protocol. Complete the table below to show, step-by-step, how to find the shortest path from each node to destination node F. Each entry in columns A through E should be of the form (NextHop, Cost).

Iteration	A	B	C	D	E

- b. Suppose the link between nodes F and E is broken (removed) after the protocol converges in part a. Show step by step how the protocol continues until it converges again.

Iteration	A	B	C	D	E

This problem has two parts. For full credit, you must answer both parts correctly.

- a. Nodes A and B are attached to opposite ends of a 100 Mbps Ethernet cable segment. Suppose A begins transmitting a frame and before it finishes, B begins transmitting a frame. For A to detect collision with B, what should be the maximum length of the Ethernet cable segment? Assume that the transmit frame size is 500 bits and signal propagation speed is  $2 \times 10^8$  m/sec. Show your work.

- b. The table below is a routing table using CIDR. Address bytes are in hexadecimal. Leading zeroes are dropped for each byte, e.g., 02 is written as 2. The notation "/12" in C4.50.0.0/12 denotes a mask with 12 leading 1 bits: FF.F0.0.0.

Prefix/Length	Next Hop
C4.50.0.0/12	A
C4.5E.10.0/20	B
C4.60.0.0/12	C
C4.68.0.0/14	D
80.0.0.0/1	E
40.0.0.0/2	F
3.0.0.0/2	G

Determine the next hop for a packet with each of the following destination addresses, assuming the match with the longest prefix is selected. Show your work.

- i. C4.6B.31.2E

- ii. 5E.43.91.12

**Problem: P36 Area: Networking, Security, and Dependability**

**Student Code:** \_\_\_\_\_

This problem has two parts. For full credit, you must answer both parts correctly.

Consider a three-person group encryption scheme based on the same principle as RSA. Suppose that some trusted entity generates two primes,  $p$  and  $q$  and forms  $n = pq$ . Now, instead of choosing a public key,  $e$ , and private key,  $d$  (as in RSA), the trusted entity chooses  $k_1, k_2$ , and  $k_3$  such that  $\gcd(k_j, n) = 1$  and  $k_1 k_2 k_3 = 1 \pmod{\phi(n)}$ .

The three users A, B, and C, respectively, are given the following keys.

A gets  $(k_1; k_2, n)$

B gets  $(k_2; k_3, n)$

C gets  $(k_1; k_3, n)$

- a. Suppose user A generates a message  $m$  such that  $\gcd(m, n) = 1$ . A wants to encrypt  $m$  so that both B and C can decrypt the ciphertext. To this end, A forms the ciphertext  $y = m^{k_1 k_2} \pmod n$ . Explain how B would decrypt  $y$ , and explain how C would decrypt  $y$ .
- b. Suppose A and B have been collaborating on some class project and have produced the message  $m$ , where  $\gcd(m, n) = 1$  again. They would like to collaborate to create a ciphertext that only C can decrypt, in a way that once  $m$  is encrypted, both A and B would have to work together to decrypt the resulting ciphertext to recover  $m$ ; neither A nor B on their own can accomplish the decryption. Explain how this can be accomplished.