Problem: CM1 **Area: Computers and Architecture** **Code #_____**

a) List and give solutions to the three types of data dependencies encountered in pipelines.

b) Identify all types of hazards present in the code below and write them using the following format: Hazard_type, Isrc , Idest . Assume no forwarding hardware is available

```
L.D     F0, 35(R1)      ; F0 ← M[R1+35]
MUL.D   F0, F0, F2      ; F0 ← F0 × F2
ADD.D   F4, F0, F0      ; F4 ← F0 + F0
DIV.D   F0, F4, F0      ; F0 ← F4 / F0
```

c) Briefly explain the process of virtual to physical address translation. Mention main components involved and steps required if a page is not present in main memory.

Problem: CM2 **Area: Computers and Architecture** **Code #_____**

Suppose we have two implementations (Machine A and machine B, namely) of the same instruction set architecture. For some program which has 1 million instructions,

Machine A has a clock cycle time of 100ps and an average CPI of 4.0.

Machine B has a clock cycle time of 130ps and an average CPI of 3.0.

a. What machine is faster for this program, and by how much?

b. If overclocking (i.e., driving the given machine with faster clock speed) of the slower machine is possible, what clock rate should be used to execute the given program to achieve the same execution time of the faster machine?

Problem: CM3 **Area: Computers and Architecture** **Code #_____**

Assume you are deciding between two possible optimizations (A and B) for a machine. Optimization A provides a speedup of 5 for 30% of the instructions, whereas Optimization B provides an increase/speedup in clock speed by 1.5%. Which optimization is a better solution? Show all work for full credit.

Problem: CM4 **Area: Computers and Architecture** **Code #_____**

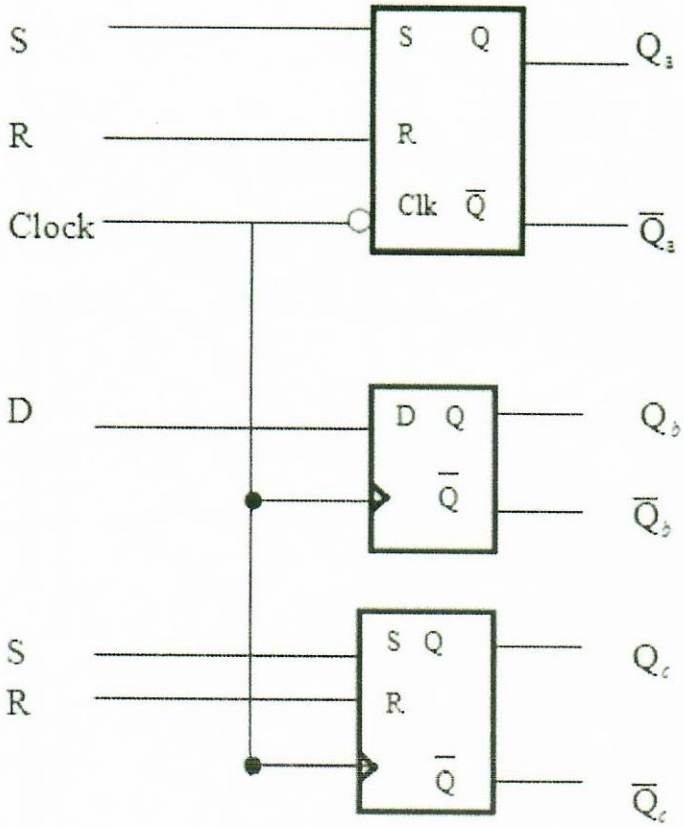
Below is a list of 32-bit memory address references, given as word addresses in decimal.

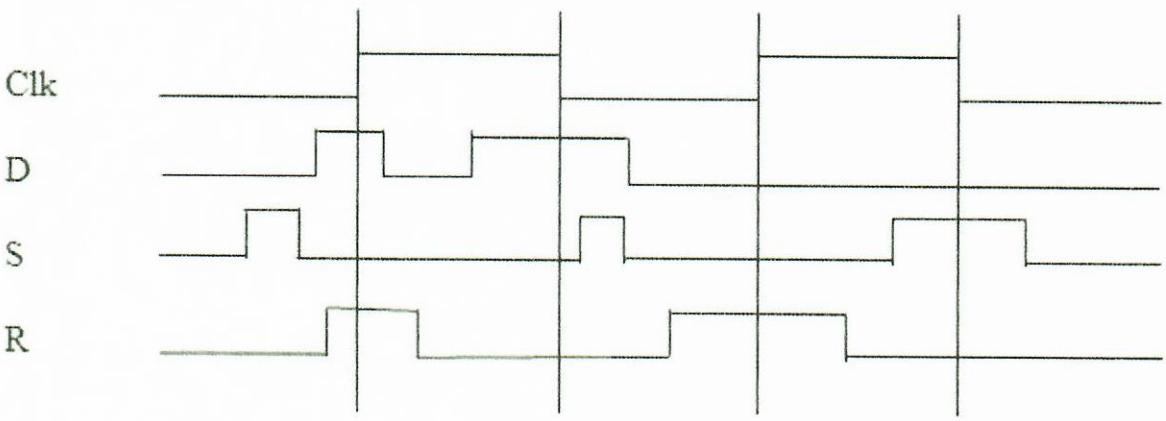
3, 180, 43, 2, 191, 88, 190, 14, 181, 44, 186, 253

For each of these references, identify the binary address, the tag, and the index given a direct-mapped cache with four-word blocks and a total size of 4 blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

Problem: CM5 **Area: Integrated Circuits and Logic Design** **Code #_____**

In the circuit below, assume an initial value of 0 for Q. Complete the timing diagram for Q_a, Q_b and Q_c.





Q_a

Q_b

Q_c

Problem: CM6 **Area: Integrated Circuits and Logic Design** **Code #_____**

Given the Boolean expression $f(a, b, c) = (\bar{a} + \bar{b})(b + \bar{c})(\overline{a + c})$ answer the following questions.

a. Simplify the following Boolean expression. *Show your work for full credit. You may use any appropriate method for simplifying the expression.*

b. Determine the truth table for f and for the simplified expression from part a. Show your work for full credit.

Given the function: $G(w,x,y,z) = \Pi(1,2,3,5,6,10,13)+dc(0,7,9,11)$

Answer the following questions.

a) Write the <u>minimal</u> SOP expression for G.

wx \ yz	00	01	11	10
00				
01				
11				
10				

b) Write the <u>minimal</u> NOR-NOR expression for G.

wx \ yz	00	01	11	10
00				
01				
11				
10				

Answer the following questions.

a) Convert to binary:
B2F (hex) =

b) Convert to binary:
592.6875 (decimal) =

c) Convert to hex:
10101101100111010.110110110 (binary) =

d) Convert –34 to 8 bit 2's complement representation.

e) Perform the 2's complement multiplication 10001111 x 01100001

f) Perform the following two's complement addition operations. Give your answer as an 8-bit two's complement number. State whether overflow occurs.

```
  1 1 0 1 0 1 1 0          0 0 1 1 0 1 1 1
+ 1 0 1 1 1 0 1 1        + 0 1 1 1 0 1 1 1
-----------------        -----------------
```

Problem: CM9 **Area: Embedded Computer Systems** **Code #_____**

a) List at least 3 advantages of programming a microcontroller using C over Assembly.

b) List at least 5 different addressing modes generally used in microcontrollers.

c) The correct choice of a microcontroller is critical in the success of a given project. Why would we still use 8-bit microcontrollers for some applications when 32-bit microcontrollers offer much better performance?

Problem: CM10 **Area: Embedded Computer Systems** **Code #_____**

a) Find the delay associated with the following code sequence. Assume you are using an 8051 system with crystal frequency of 11.0592 MHz and 12 cycles/Machine Cycle. The number of machine cycles for type of instruction are as follows:

MOV = 1, NOP = 1, INC = 1, DJNZ = 2 (decrements value by 1 and jumps to label if value is not zero)

```
            MOV A, #1
DELAY:      MOV R7, #50
LOOP3:      MOV R6, #50H
LOOP2:      MOV R5, #00010100B
LOOP1:      NOP
            INC A
            NOP
            DJNZ R5, LOOP1
            DJNZ R6, LOOP2
            DJNZ R7, LOOP3
```

b) Explain the difference between CISC and RISC microcontrollers and list advantages of each type.

a) Describe how a typical embedded processor (e.g. 8051, ARM) handles interrupts? What is the procedure of calling the interrupt service routing (ISR) after an interrupt signal is generated?

b) How the processor state is saved and restored during the interrupt handling procedure? Which tasks are handles automatically and which require software support? Note: You can either discuss generic case or use one of the typical processors (e.g. 8051, ARM) as an example.

Problem: CM12 **Area: Embedded Computer Systems** **Code #_____**

Consider a timer 0 in 8051 type processor with hardware configuration and control registers shown on the attached figures and tables. Assume following: SYSCLOCK = 12MHz, External Clock (T0) = 1MHz

a) Explain how the timer 0 operates in Mode 2 (timer/counter with auto-reload).

b) Consider that the timer should overflow (timeout) every 1ms. Which clock source can you use – either SYSCLK or External Clock (T0) – to achieve this timeout? What reload value should be used? Note: The SYSCLK signal can be pre-scaled before driving the timer (slowed down).

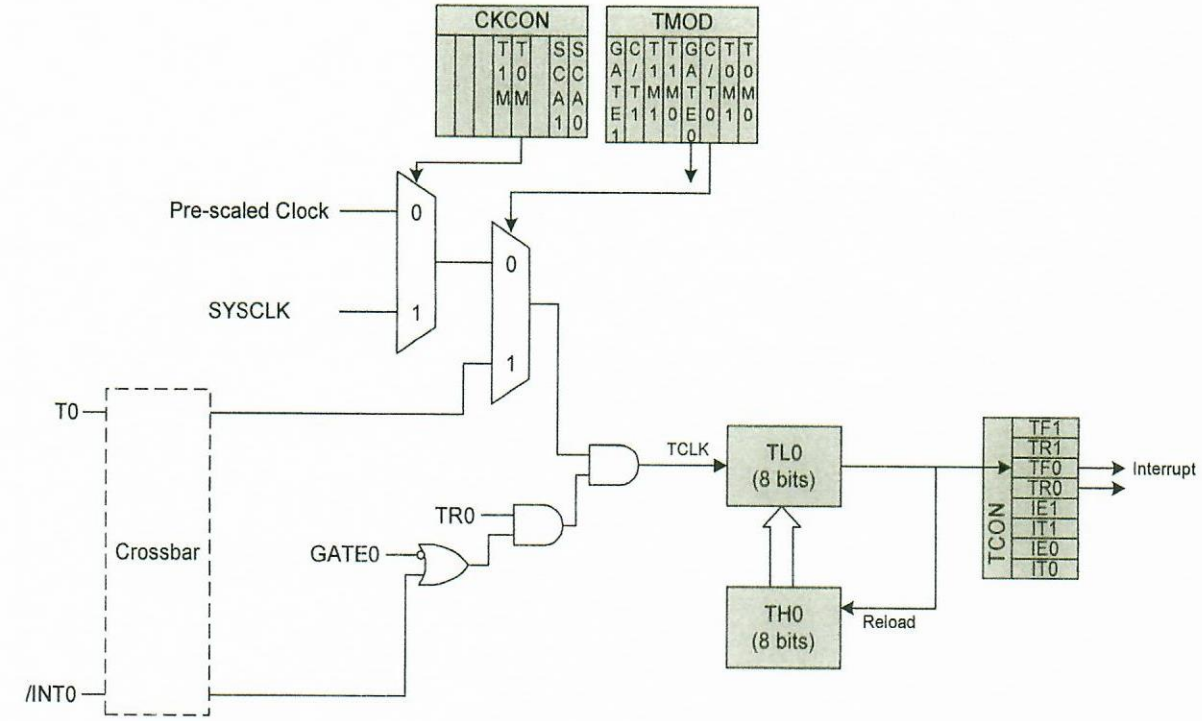


Figure 23.2. T0 Mode 2 Block Diagram

SFR Definition 23.1. TCON: Timer Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Bit Addressable

SFR Address: 0x88
SFR Page: 0

Bit7: TF1: Timer 1 Overflow Flag.
Set by hardware when Timer 1 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 1 interrupt service routine.
0: No Timer 1 overflow detected.
1: Timer 1 has overflowed.

Bit6: TR1: Timer 1 Run Control.
0: Timer 1 disabled.
1: Timer 1 enabled.

Bit5: TF0: Timer 0 Overflow Flag.
Set by hardware when Timer 0 overflows. This flag can be cleared by software but is automatically cleared when the CPU vectors to the Timer 0 interrupt service routine.
0: No Timer 0 overflow detected.
1: Timer 0 has overflowed.

Bit4: TR0: Timer 0 Run Control.
0: Timer 0 disabled.
1: Timer 0 enabled.

Bit3: IE1: External Interrupt 1.
This flag is set by hardware when an edge/level of type defined by IT1 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 1 service routine if IT1 = 1. This flag is the inverse of the /INT1 signal.

Bit2: IT1: Interrupt 1 Type Select.
This bit selects whether the configured /INT1 interrupt will be falling-edge sensitive or active-low.
0: /INT1 is level triggered, active-low.
1: /INT1 is edge triggered, falling-edge.

Bit1: IE0: External Interrupt 0.
This flag is set by hardware when an edge/level of type defined by IT0 is detected. It can be cleared by software but is automatically cleared when the CPU vectors to the External Interrupt 0 service routine if IT0 = 1. This flag is the inverse of the /INT0 signal.

Bit0: IT0: Interrupt 0 Type Select.
This bit selects whether the configured /INT0 interrupt will be falling-edge sensitive or active-low.
0: /INT0 is level triggered, active logic-low.
1: /INT0 is edge triggered, falling-edge.

SFR Definition 23.2. TMOD: Timer Mode

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
GATE1	C/T1	T1M1	T1M0	GATE0	C/T0	T0M1	T0M0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x89
SFR Page: 0

Bit7: GATE1: Timer 1 Gate Control.
0: Timer 1 enabled when TR1 = 1 irrespective of /INT1 logic level.
1: Timer 1 enabled only when TR1 = 1 AND /INT1 = logic 1.

Bit6: C/T1: Counter/Timer 1 Select.
0: Timer Function: Timer 1 incremented by clock defined by T1M bit (CKCON.4).
1: Counter Function: Timer 1 incremented by high-to-low transitions on external input pin (T1).

Bits5–4: T1M1–T1M0: Timer 1 Mode Select.
These bits select the Timer 1 operation mode.

T1M1	T1M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Timer 1 inactive

Bit3: GATE0: Timer 0 Gate Control.
0: Timer 0 enabled when TR0 = 1 irrespective of /INT0 logic level.
1: Timer 0 enabled only when TR0 = 1 AND /INT0 = logic 1.

Bit2: C/T0: Counter/Timer Select.
0: Timer Function: Timer 0 incremented by clock defined by T0M bit (CKCON.3).
1: Counter Function: Timer 0 incremented by high-to-low transitions on external input pin (T0).

Bits1–0: T0M1–T0M0: Timer 0 Mode Select.
These bits select the Timer 0 operation mode.

T0M1	T0M0	Mode
0	0	Mode 0: 13-bit counter/timer
0	1	Mode 1: 16-bit counter/timer
1	0	Mode 2: 8-bit counter/timer with auto-reload
1	1	Mode 3: Two 8-bit counter/timers

SFR Definition 23.3. CKCON: Clock Control

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
-	-	-	T1M	T0M	-	SCA1	SCA0	00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8E
SFR Page: 0

Bits7–5: UNUSED. Read = 000b, Write = don't care.

Bit4: T1M: Timer 1 Clock Select.
This select the clock source supplied to Timer 1. T1M is ignored when C/T1 is set to logic 1.
0: Timer 1 uses the clock defined by the prescale bits, SCA1–SCA0.
1: Timer 1 uses the system clock.

Bit3: T0M: Timer 0 Clock Select.
This bit selects the clock source supplied to Timer 0. T0M is ignored when C/T0 is set to logic 1.
0: Counter/Timer 0 uses the clock defined by the prescale bits, SCA1-SCA0.
1: Counter/Timer 0 uses the system clock.

Bit2: UNUSED. Read = 0b, Write = don't care.

Bits1–0: SCA1–SCA0: Timer 0/1 Prescale Bits
These bits control the division of the clock supplied to Timer 0 and/or Timer 1 if configured to use prescaled clock inputs.

SCA1	SCA0	Prescaled Clock
0	0	System clock divided by 12
0	1	System clock divided by 4
1	0	System clock divided by 48
1	1	External clock divided by 8*

***Note:** External clock divided by 8 is synchronized with the system clock, and external clock must be less than or equal to the system clock frequency to operate the timer in this mode.

SFR Definition 23.4. TL0: Timer 0 Low Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8A
SFR Page: 0

Bits 7–0: TL0: Timer 0 Low Byte.
The TL0 register is the low byte of the 16-bit Timer 0.

SFR Definition 23.6. TH0: Timer 0 High Byte

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Reset Value
								00000000
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

SFR Address: 0x8C
SFR Page: 0

Bits 7–0: TH0: Timer 0 High Byte.
The TH0 register is the high byte of the 16-bit Timer 0.

Problem: CM14 **Area: Computational Intelligence** **Code #_____**

Compare and contrast, using math and your explanations, Heuristic Dynamic Programming vs. Q learning.

Problem: CM16 **Area: Computational Intelligence** **Code #_____**

Describe how an evolutionary algorithm can be enhanced to deal well with multiobjective optimization.

Problem: CM17 **Area: Networking** **Code** _____

Answer <u>all three</u> questions below.

1. List all the layers of the TCP/IP protocol suite and briefly describe the functions of each layer. Give an example protocol for each layer.

2. List three advantages of packet-switched networks over circuit-switched networks and justify your choices.

3. List three reasons why bridges are used in interconnecting multiple LANs.

Problem: CM18 **Area: Networking** **Code** _____

Answer <u>all three</u> questions below. Show every step of your work.

1. Calculate the total delay to transfer a 10 Mb file from host 1 to host 2. This delay spans the beginning through the time when host 2 receives the last bit of the file. Circuit switching is used.

   Assume the following parameters:

   - The distance between the two hosts is 4000 km.
   - There are three routers between the hosts. These routers divide the distance between the two hosts into four equal parts.
   - Propagation speed is 200,000 km/s.
   - Transmission data rate is 100 Kbps.
   - Router processing delay is 100 ms.
   - Processing delays in hosts is negligible.

2. Repeat part 1, this time assuming datagram switching with a datagram size of 65 Kb.

3. Which switching technique yielded less delay? Comment on this result.

Problem: CM19 **Area: Networking** **Code**

Assume that a router has built up the routing table shown below. The router can deliver packets directly over interfaces 0 and 1, or it can forward packets to routers R2, R3, or R4.

Subnet Number	Subnet Mask	Next Hop
128.96.39.0	255.255.255.128	Interface 0
128.96.39.128	255.255.255.128	Interface 1
128.96.40.0	255.255.255.128	R2
192.4.153.0	255.255.255.192	R3
(default)		R4

Describe what the router does with a packet addressed to each of the destinations below. Justify your answers. You may find the following decimal-to-hex conversions useful:

90D = 5AH, 128D = 80H, 192D = C0H, 153D = 99H.

(a) 128.96.39.10
(b) 128.96.40.12
(c) 128.96.40.151
(d) 192.4.153.17
(e) 192.4.153.90

Problem: CM20 **Area: Networking** **Code**

Answer both questions below.

1. Describe the factors that should be considered in deciding between error detection and error correction, and provide a practical example where error correction is preferable.

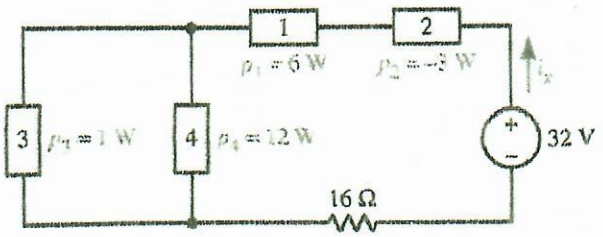
2. We want to design a code with m message bits and r check bits that will allow all single-bit errors to be corrected.

   Derive an inequality that will allow you to determine the minimum value of r for a given m.

   You do not have to solve for a closed-form solution of r. Presenting the inequality will suffice, assuming that you show the work leading to the inequality.

Problem M5 Circuits/Electronics Code #_____

Referring to the right network with power (in watts) and resistor (in ohms) values specified in the elements of the figure, determine the value of i_x



Problem #M11 **Area: Waves & Devices Code #**

Consider a silicon (Si: a Col. IV material)) abrupt-junction pn diode in which only donors are on the n-side and only acceptors are on the p-side. T = 300 K. Important physical constants are:

Boltzmann's constant: $k = 1.38 \times 10^{-23}$ J/K = 8.62×10^{-5} eV/K

Planck's constant: $h = 4.14 \times 10^{-15}$ eV-s Electronic charge: $q = 1.60 \times 10^{-19}$ C

Carrier Mobilities $\mu_n = 1350$ cm^2/V-s $\mu_p = 480$ cm^2/V-s

Bandgap Energy of Si $E_g = 1.11$ eV

Intrinsic Carrier Concentration $n_i = 1.50 \times 10^{10}$ cm^{-3} at 300 K

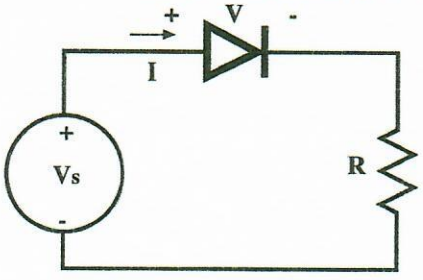
(a) Silicon (Si) is a column IV material on the periodic table and it is in the third row. Neon (Ne) is a column VIII material on the periodic table and it is at the end of the second row. If the electronic configuration for Neon is $1s^2 2s^2 p^6$, state the electronic configuration for Silicon.

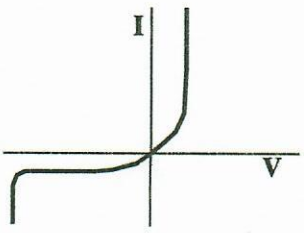
(b) Name the type of mobile carriers that are found in the listed energy bands.

Energy band	Mobile Carriers (electrons or holes)
Valence Band:	_____
Conduction Band:	_____

(c) The contact potential is $V_o = 0.70$ V. Calculate the doping concentrations for the p and n sides if the doping concentrations on each side are equal. .

(d) Let the turn-on voltage be $V_{to} = 0.70$ V, the reverse saturation current be 0.50 mA, and the breakdown voltage be –15 V in the characteristic below. Calculate the most negative current I if R = 2,000 Ω and $V_S = +20 \sin(10t)$ V.





Problem M-21 Communications/Signal Processing Code# _____

I find a black box on a laboratory bench. The box has one connection marked "input" and one connection marked "output". It is impossible to see what is contained in the box. It rattles a little when shaken, and feels a little bit heavier on the output end than it does on the input end. The center of the box is distinctly warmer than either end, although I can easily touch it anywhere without getting burned. It seems to hum slightly, and I've been told it glows dark red at night, but the glow is not visible with the laboratory lights on.

I test the box by connecting the input to a voltage source that produces and ideal Dirac delta function, $\delta(t)$. The output I connect to an oscilloscope, and observe that it looks like $-10e^{-5t}u(t)$, where $u(t)$ is the unit step function. Based on this measurement, and the observations above – but making no other assumptions about the box, tell me what output you will observe when each of the two signals listed below is put on the input by an ideal voltage source. If you think there is insufficient information provided to answer this question, explain what else you would need before you could answer these questions.

A) Input is $-9\delta(t-7)$ volts

B) Input is $15.5 \cos(2\pi 800t+800)$ volts

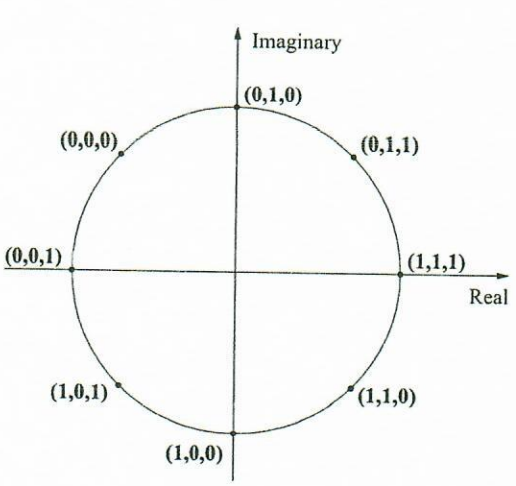
A communication system employs the Gray code and 8-PSK passband modulation scheme. The constellation of the modulated signals and their corresponding Gray codes are shown in Figure 2(a). To achieve better bandwidth efficiency, the system also employs square-root raised cosine filter with a roll-off factor of 0.30 as the transmit pulse shaping filter and receive matched filter. The received signal is coherently demodulated and the matched filter output is a complex signal $s(t)$, as shown in Figure 2(b). Answer the questions according to the figures.

1. What does PSK stand for? How many orthonormal base functions does PSK employ and what are they?

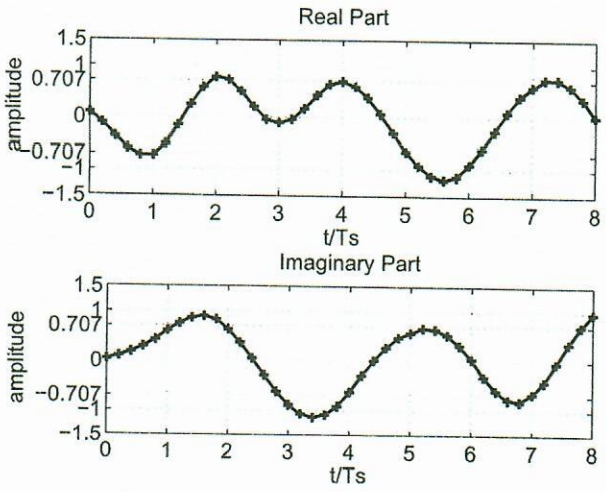
2. What is the Maximum Likelihood (ML) decision rule? Explain and show the decision regions on the constellation plot (Figure 2(a)) using one symbol as an example.

3. What are the values of the complex symbols $s(k)$ for $k = t/T_s = 3, 4, 5, 6$ (symbols). Show your reasoning by indicating them in Figure 2(b).

4. Decode the symbols for $k = 3, 4, 5, 6$ to binary bit stream using the ML rule and the Gray Code constellation plot Fig. 2(a).



(a) Gray code and 8-PSK modulation.



(b) The output of the receive matched filter: $s(t)$.

Figure 2: Figures for Problem IV