Problem: CM1 **Area: Computers and Architecture** **Code #_________**

Design an 8-bit ripple carry adder which can be used for addition and subtraction operation. In addition to input words and output word, your design should have a carryout bit and one select bit to select either addition operation or subtraction operation. You are allowed to use full adder and logic gates to design it.

Problem: CM2 **Area: Computers and Architecture** **Code #________**

Find the average memory access time (AMAT) for a processor with a 1ns clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction, and a cache access time (including hit detection) of 1 clock cycle. Assume that the read and write miss penalties are the same and ignore other write stalls.

Problem: CM3 **Area: Computers and Architecture** **Code #________**

Suppose we have two implementations (Machine A and machine B, namely) of the same instruction set architecture. For some program which has 1 million instructions,

Machine A has a clock cycle time of 100ps and an average CPI of 4.0.

Machine B has a clock cycle time of 130ps and an average CPI of 3.0.

a. What machine is faster for this program, and by how much?

b. If overclocking (i.e., driving the given machine with faster clock speed) of the slower machine is possible, what clock rate should be used to execute the given program to achieve the same execution time of the faster machine?

Problem: CM4 **Area: Computers and Architecture** **Code #________**

Suppose the following MIPS instruction sequence gets executed on the basic five-stage pipeline MIPS processor.

```
lw $5, 0($5)
add $5, $5, $5
sw $5, 0($5)
```

a. Assume there is no forwarding in this pipelined processor. Indicate hazards and add nop instructions (if needed) to eliminate them. Clearly justify your answer.

b. Assume there is full forwarding (EXE forwarding and MEM forwarding). Indicate hazards and add nop instructions (if needed) to eliminate them. Clearly justify your answer.

Problem: CM5 **Area: Integrated Circuits and Logic Design** **Code #_________**

Implement the function $g(a, b, c) = b'c + ac$ based on the approaches in parts **a** and **b** below.

a) Using an 8:1 multiplexer

b) Using a 3:8 decoder with active high outputs

c) Using a 3:8 decoder with active low outputs

Problem: CM6 **Area: Integrated Circuits and Logic Design** **Code #_________**

Given the state table below with the state variables X and Y, externally applied input r, and output f. Answer the questions below.

Present Input	Present State		Present Output	Next State		JK Flip Flop Inputs		SR Flip Flop Inputs	
r	X	Y	f	X*	Y*	J_X	K_X	S_Y	R_Y
0	0	0	0	0	1				
0	0	1	1	1	0				
0	1	0	0	0	0				
0	1	1	1	1	1				
1	0	0	1	0	1				
1	0	1	1	0	0				
1	1	0	0	1	1				
1	1	1	0	1	0				

a) Fill in the missing values for the state table.
b) Draw the state transition diagram based on the state table.

Problem: CM7 **Area: Integrated Circuits and Logic Design** **Code #__________**

Given the function: F(w,x,y,z) = Σm(0,1,2,3,4,6,7,8,10,13)+dc(9,11,14)

Answer the following questions.

a) Write the <u>minimal</u> POS expression for F.

wx \ yz	00	01	11	10
00				
01				
11				
10				

b) Write the <u>minimal</u> SOP expression for F.

wx \ yz	00	01	11	10
00				
01				
11				
10				

c) Determine the implementation for F that uses the fewest number of logic gates (AND, OR, INVERTERS, NAND, NOR up to 3 inputs).

Problem: CM8 **Area: Integrated Circuits and Logic Design** **Code #_________**

Answer the questions for parts **a** and **b** below.

a) Simplify the following Boolean expression using Boolean algebra:

$f(w,x,y,z) = (w + x' + z)(x + y' + z')(w + y' + z)(w' + x' + y' + z')$

b) Simplify the following Boolean expression using Boolean algebra:

$f(a,b,c) = ((a+bc+a'c)(a'+c'))'$

Problem: CM9 **Area: Embedded Computer Systems** **Code #________**

List and explain the basic 6 addressing modes employed in micro-controllers. You can discuss them in context of a specific architecture (e.g. 8051, ARM).

Problem: CM10 **Area: Embedded Computer Systems** **Code #________**

Assume that you have an 8051 microcontroller with a 12 MHz operation. Write an assembly language program to create a 83.3 kHz square wave on P1.0. Timers or interrupts are not required for this assembly language program. Show your work for the timing involved for: 1) executing each instruction and 2) generating the time delay associated with the 83.3 kHz square wave.

Problem: CM11 **Area: Embedded Computer Systems** **Code #________**

Low -level programming is still an important way to optimize performance in embedded devices. For this problem, fully explain how low-level instruction sets handle various required programming features found in high-level languages. When possible, use specific examples from instruction sets you may know. Include relevant architectural details when appropriate.

(a) arrays

(b) function calls

(c) conditionals

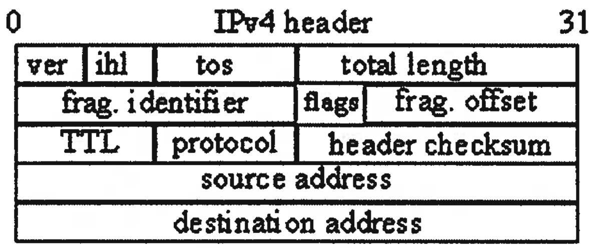
Problem: CM12 **Area: Embedded Computer Systems** **Code #________**

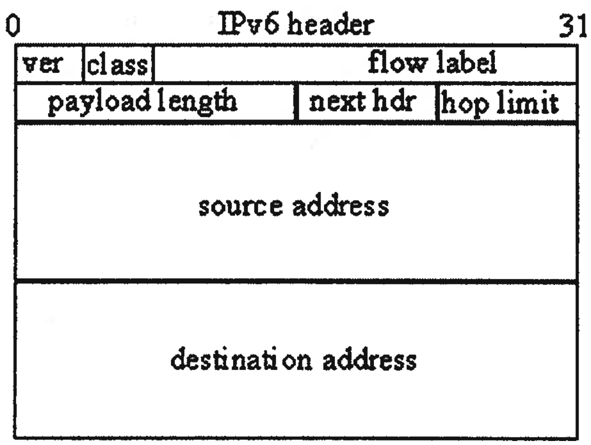
(a) Sketch the datapath diagram for a generic UART. Indicate inputs, outputs, and label the components.

(b) Detail the steps involved in configuring a UART to send data to a receiving device.

Problem: CM18 **Area: Networking** **Code ________**

Enumerate and discuss the differences between IPv4 and IPv6. You can utilize the attached header formats to make comparison.





Problem: CM19 **Area: Networking** **Code ________**

Explain and compare the basic automatic reply queuing (ARQ) techniques: stop-and-wait and sliding window. Give example systems or protocols that employ each.

Problem: CM20 **Area: Networking** **Code ________**

In the context of signal encoding, answer all of the following questions:

1. Briefly describe the operation of quadrature phase shift keying (QPSK). Which features of the signal are being manipulated?

2. Describe one advantage and one disadvantage of QPSK as compared to binary phase shift keying (BPSK).

3. Describe one advantage and one disadvantage of QPSK as compared to quadrature amplitude modulation (QAM-16).

4. In a given communication scenario, the bit rate achieved is 8 kbps. The baud rate used is 1 kbaud. Draw a constellation diagram that could represent the signal encoding. Explain your answer. This question has more than one correct answer.

Problem: CM21 **Area: Security & Reliability** **Code #_________**

Answer <u>all five of the questions below.</u>

1. Describe the difference between an unconditionally secure cipher and a computationally secure cipher.

2. Are any known ciphers unconditionally secure? If so, name and describe the method(s), and explain why computationally secure ciphers are still used despite the existence of superior methods.

3. Define diffusion and confusion (in the context of encryption), respectively, and explain the difference between the two.

4. Suppose H(m) is a collision-resistant hash function that maps a message of arbitrary bit length into an n-bit hash value. Is it true that: for all messages x, x' with $x \neq x'$, we have $H(x) \neq H(x')$? Justify your answer.

5. Precisely define reliability and availability, respectively, and explain the difference between the two.

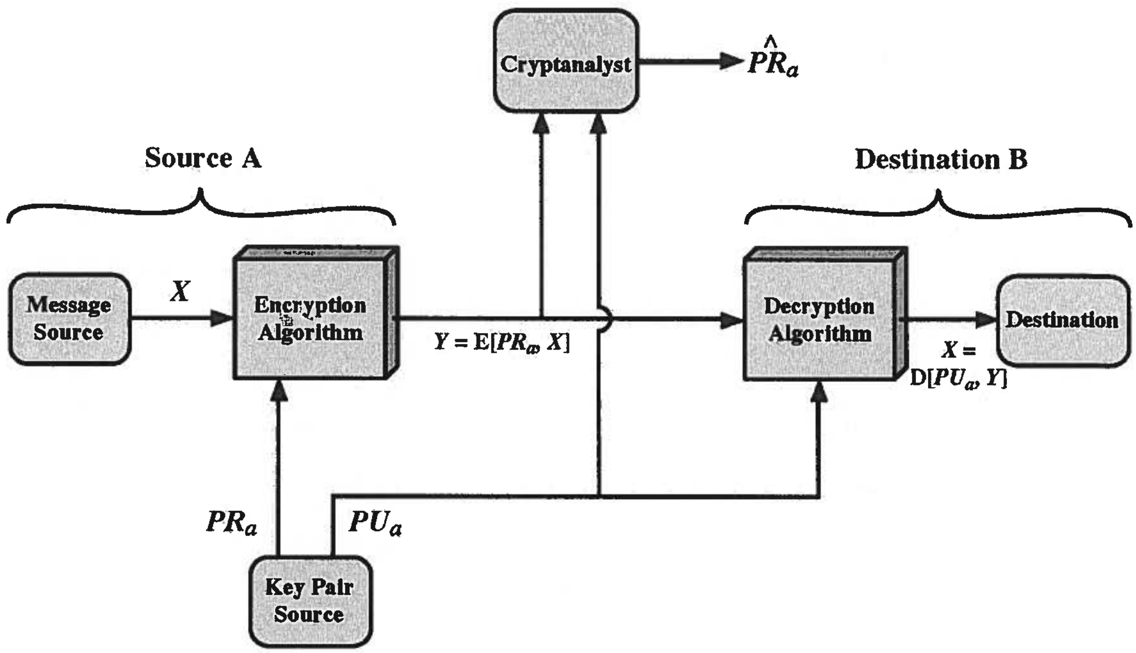
Problem: CM22 **Area: Security & Reliability** **Code #________**

This problem illustrates a simple application of the chosen ciphertext attack. Bob intercepts a ciphertext, C, intended for Alice and encrypted with Alice's public key, e. Bob wants to obtain the original message, $M = C^d \bmod n$. Bob chooses a random value r, less than n, and computes:

$$Z = r^e \bmod n$$
$$X = ZC \bmod n$$
$$t = r^{-1} \bmod n$$

Next, Bob gets Alice to authenticate (sign) X with her private key (as in the figure below), thereby decrypting X. Alice returns $Y = X^d \bmod n$.

Show (mathematically) how Bob can use the information now available to him to determine M.



Problem: CM23 **Area: Security & Reliability** **Code #________**

a. At least, how many components should be arranged in parallel (i.e., at least one component should be fault-free) to build a system to achieve Rsystem(200) ≥ 0.95?

b. If the system is modified so that at least 2 fault-free components are required to be functional out of n components where n ≥ 2, determine minimum n that satisfies Rsystem(44) ≥ 0.88. Note n should be an integer value since it is the number of components.

Problem: CM24 **Area: Security & Reliability** **Code #________**

Determine the following.

a. A Cyclic Code word is received as 1011110 which may or may not be erroneous. Determine if the received Cyclic code word is valid or invalid using G(X) = x3 + x + 1.

b. Find the Cyclic Code word for information word 1100 using G(X) = x3 + x + 1.

Problem: CM25 **Area: Computer Science** **Code #________**

Prove, formally, whether the following are True or False; show your work.

$\log_2 n$ is $O(\log_3 n)$

$\sum_{1}^{n} 5ni$ is $\Theta(n^3)$

Problem: CM26 **Area: Computer Science** **Code #________**

Prove by mathematical induction that $\forall n \in Z, n \geq 4, n! > n^2$

Problem: CM27 **Area: Computer Science** **Code #________**

True or False, explain your answer for each for full credit.

a. An algorithm can always be computed by a computer.

b. Hard problems, such as the traveling salesperson problem, in Computer Science are those that are difficult to understand and express easily.

c. A loop invariant is true before the loop starts, at the start of each execution of the loop, and right up until the moment when the loop is exited, and then the post condition becomes true.

d. If f(n) is $\Theta(g(n))$, then f(n) is $O(g(n))$ and f(n) is $\Omega(g(n))$.

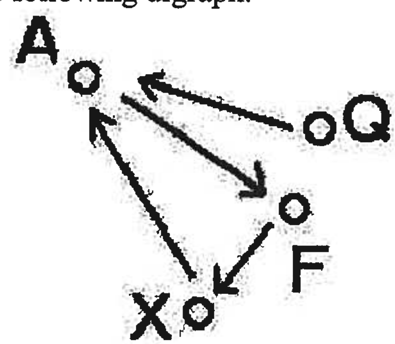
e. The halting problem addresses techniques to debug algorithms.

Problem: CM28 **Area: Computer Science** **Code #_________**

Cycles in a digraph.

a. Write code to determine if a directed graph has a cycle. Use either Depth First Search or Breadth First Search.

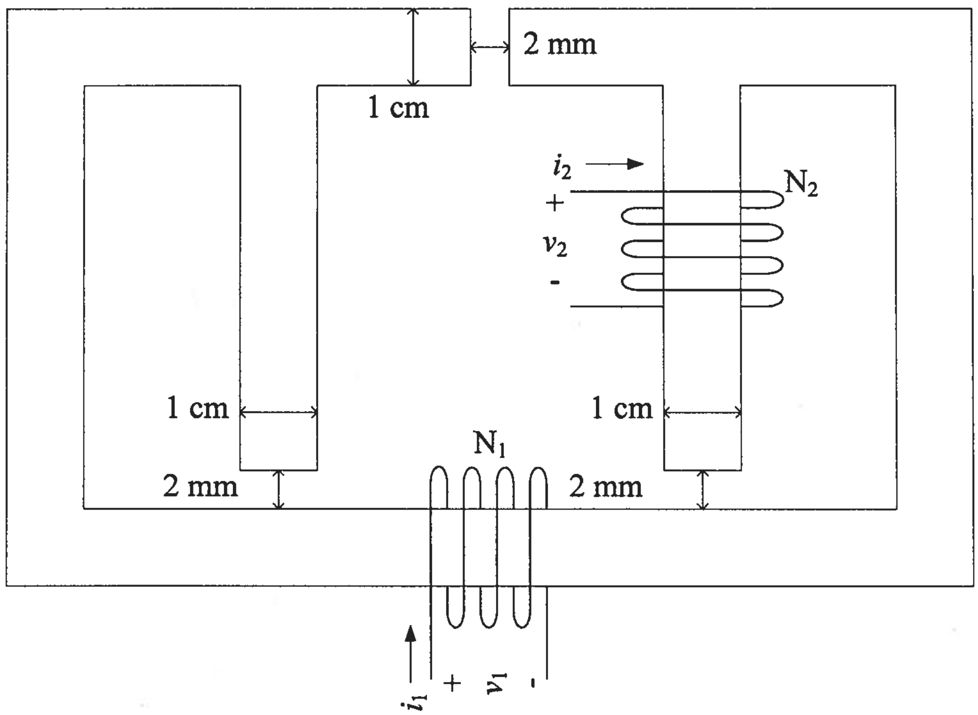
b. Show an example of your algorithm's execution on the following digraph.



c. Formulate an invariant that describes what portion of the graph has been explored so far at each step of the execution.

Problem M.1 **Power/Machinery** **Code #_________**

Consider the magnetic structure drawn below. The steel has infinite permeability. Depth into the page is 1.5 cm. All air gaps are the same dimensions: 1 cm wide, 2 mm long. N1 = 300, N2 = 100.



a. Draw the magnetic equivalent circuit. Mark all polarities, and find all reluctances numerically.
b. Determine the inductance matrix for the device that relates λ_1 and λ_2 to i_1 and i_2.

Problem M.2 **Power/Machinery** **Code #_________**

A particular machine has the following λ-i relationship:

$$\begin{bmatrix} \lambda_1 \\ \lambda_2 \\ \lambda_3 \end{bmatrix} = \begin{bmatrix} L_0 & L_1 & L_2 \cos 2\theta \\ L_1 & L_0 & L_2 \sin 2\theta \\ L_2 \cos 2\theta & L_2 \sin 2\theta & L_3 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix}$$

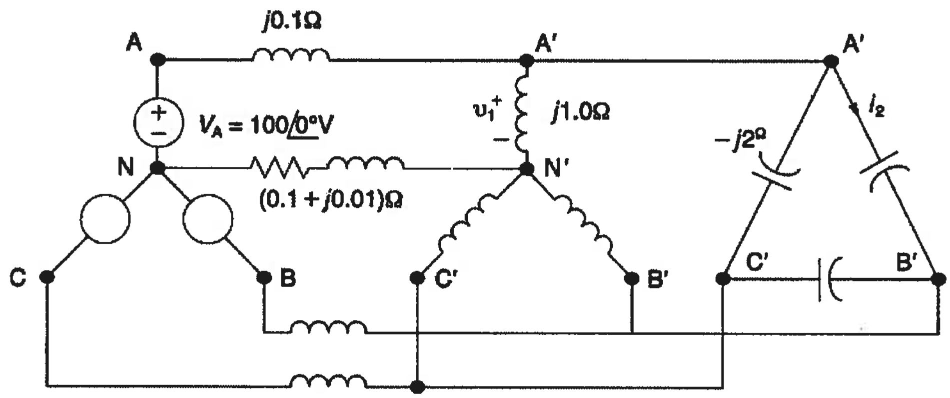
where L_0, L_1, L_2, and L_3 are constant, and θ is the position variable for the rotor. For parts c & d, suppose $i_1 = \sqrt{2} I_s \cos(\omega_e t)$, $i_2 = \sqrt{2} I_s \sin(\omega_e t)$, $i_3 = I_f$, $\theta = \omega_m t + \phi$. Useful identities:

$$\sin(A \pm B) = \sin A \cos B \pm \cos A \sin B$$
$$\cos(A \pm B) = \cos A \cos B \mp \sin A \sin B$$

a. Find the co-energy $W'_{fld}(i_1, i_2, i_3, \theta)$.
b. Find the torque $T_{fld}(i_1, i_2, i_3, \theta)$.
c. Determine the relationship between ω_e and ω_m such that the torque is no longer a function of time.
d. For frequencies that satisfy (c), determine the average torque $T_{ave}(I_f, I_s, \phi)$.

Problem M.3 **Power/Machinery** **Code #__________**

Calculate the power delivered by the 3-phase source for the following system (sources, lines, and loads are balanced):



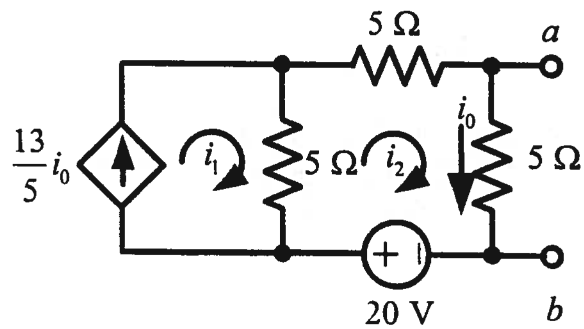
Problem M.4 **Power/Machinery** **Code #_________**

A three phase 100kV (L-N) Y-connected motor consumes 60MW at a power factor of 0.8 lagging. If this motor is connected to a three phase Y-connected voltage source using a transmission line with a transmission matrix of T, what is the phase current of the source?

$$T = \begin{bmatrix} 0.99 & 0.2\angle 80^\circ \\ 0.001\angle 90^\circ & 0.99 \end{bmatrix}$$

Prob. M5 **Area: Circuits/Electronics** **Code # _______**

Determine the Thevenin Voltage and Thevenin Resistance for the circuit below.



For the following circuit, find R, I, and a. All transformers and components should be assumed to be ideal.