Computer Engineering 2210 Final

Name	

11 problems, 100 points.

Closed books, closed notes, no calculators. You would be wise to read all problems before beginning, note point values and difficulty of problems, and budget your time accordingly.

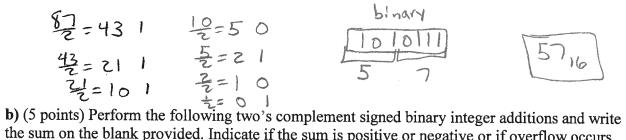
Please do not open the test until I tell you to do so.

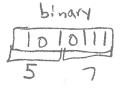
Good luck!

Question	Total Possible	Test Score
1	9	
2	6	
3	10	
4	14	
5	5	
6	6	
7	12	
8	7	
9	10	
10	15	
11	6	
Total	100	

Problem 1

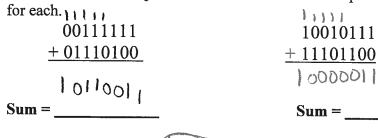
a) (2 points) Convert the given decimal number into its binary and then hexadecimal values.







the sum on the blank provided. Indicate if the sum is positive or negative or if overflow occurs



Sign of sum? Positive (Negative



Sign of sum? Positive Negative



Overflow?



NO

Overflow?



c) (2 point) Find 8-bit 2's complement of 001110112 and its associated decimal equivalent value.

Problem 2) (6 Points) Simplify the following Boolean expression:

$$f(x,y,z) = (\overline{x+z})(\overline{x+y})(\overline{y+z})$$

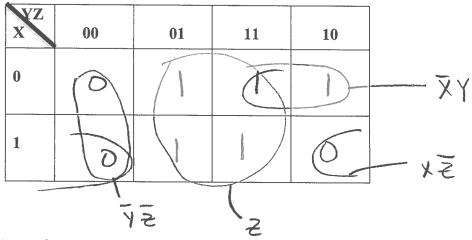
Show your work for full credit. You can use any appropriate method for simplification.

Problem 3) For the Boolean function f(x,y,z) described by the following table, give the required forms:

<u>x</u>	Y	Z	<u>f</u>
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

(2 points) Canonical Product-of-Sum expression =
$$(X+Y+Z)(X+Y+Z)(X+Y+Z)$$

Use the following K-map to calculate the minimal Sum-of-Product and minimal Product-of-Sum for the function f:



(3 points) Minimal Sum-of-product expression =

(3 points) Minimal Product-of-sum expression =

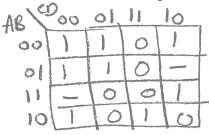
Problem 4)

Consider the following logic function and answer the questions below:

$$F(A, B, C, D) = \Sigma m(0,1,2,4,5,8,11,14) + dc(6,12)$$

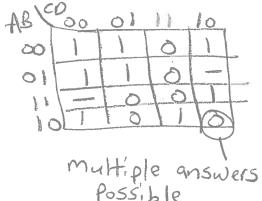
Note dc(6,12) means minterms 6 and 12 are don't care conditions.

a. (2 points) Construct a K-map of this function.



b. (3 points) Calculate minimal (minimum) Sum-of-Product (SOP) form of the given function from its K-map. \overline{A}

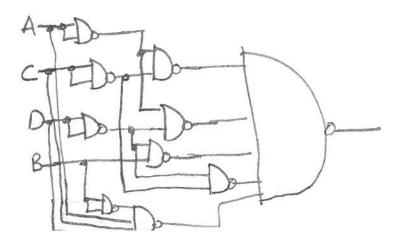
c. (5 points) Find minimal (minimum) NAND-NAND logic function of F.



$$F = \overline{Ac} + \overline{AD} + \overline{BD} + \overline{cD} + \overline{ABcD}$$

$$F = (\overline{Ac}) (\overline{AD}) (\overline{BD}) (\overline{cD}) (\overline{ABcD})$$

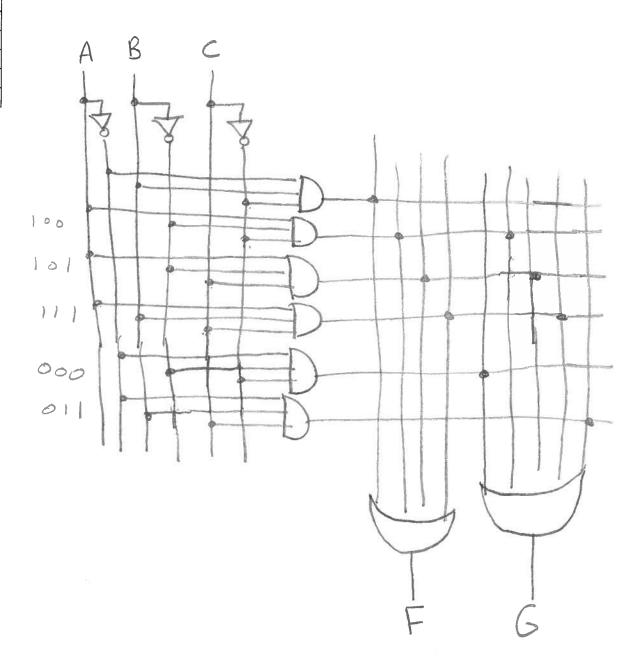
d. (3 points) Then, draw a logic diagram of the minimal (minimum) NAND-NAND logic function obtained in part c.



Problem 5)

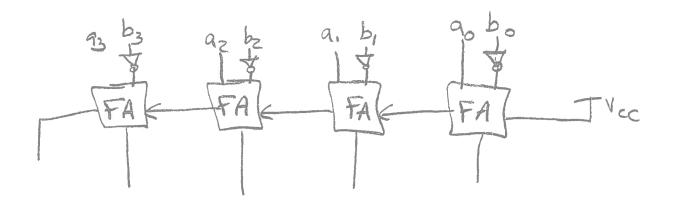
(5 points) Draw the AND-OR PLA (Programmable Logic Array) for the functions F(A,B,C) and G(A,B,C) represented in the following truth table.

ABC	F	G
000	0	1
001	0	0
010	1	0
011	0	1
100	1	:1
101	1	×1
110	0	0
111	1	-1



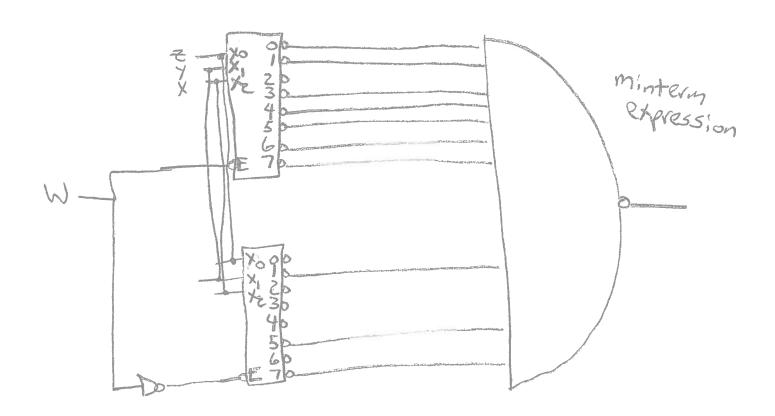
Problem 6)

(6 points) Design a 4-bit ripple-carry adder using full adders (FAs) and logic gates to generate the function A-B, where A and B are 2's complement signed words ($A = a_3a_2a_1a_0$ and $B=b_3b_2b_1b_0$, namely), and produces the sum (difference) and carry-out outputs.

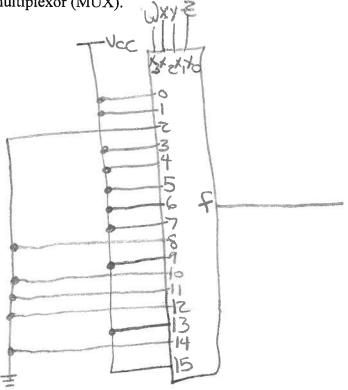


Problem 7)

a) (7 points) Show how to connect two 3:8 decoders with active-low outputs and active-low enable signals to implement the four-variable function $f(w,x,y,z) = \Sigma m(0,1,3,4,5,6,7,9,13,15)$. You may use a single NOT gate and a single NAND gate in addition to the decoders.



b) (5 points) Show how to implement the function $f(w,x,y,z) = \sum m(0,1,3,4,5,6,7,9,13,15)$ using a 16:1 multiplexor (MUX).



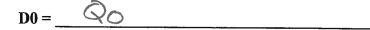
Problem 8)

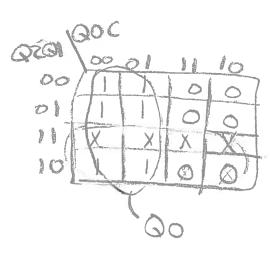
(7 points) Design a binary mod-6 up/down counter. Note the smallest count is 000 and the largest is 101 in binary. If the input C=0, count up, and if C=1, count down. When counting down from 000, it rolls back to 110 in binary. When counting up from 101, it also rolls back to 000 in binary. Use "don't cares" for unused states. Fill in the truth table and calculate the next-state logic for the LSB (Least Significant Bit) of the state. Use DFF's (D-type Flip-Flop) for the state memory.

Truth Table								
Present Count			Input	Next Count				
Q2	Q1	Q0	С	Q2* Q1		Q0*		
0	0	0	0	0	٥	1		
		U	1		0	1		
0	0	1	0	0)	0		
	0	1	1	Ó	9	O		
0	1	0	0	5	-	1		
			1	ව	0			
0	1	1	0)	0	0		
			1	0		٥		
1	n	$0 \mid 0$	0	1	0	1		
			1	_ 6	1			
1	n	0 1	0	0	0	0		
	U		1	- Sx	0	0		
1	1	1 0	0	X	X	X		
			1	X	X	χ		
1	1	$\begin{bmatrix} 1 & 1 \end{bmatrix}$	0	X	Х	X		
					1	X	×	×

Next State Logic

DO=00*



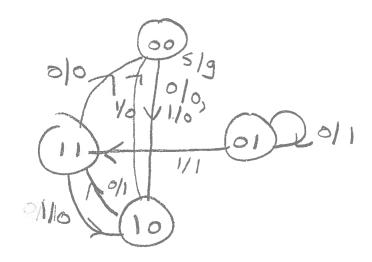


Problem 9)

Given the state table below with the state variables A and B, externally applied input s, and output g. Answer the questions below.

Present Input	Present State		Present Output	Next State		JK Flip Flop Inputs		SR Flip Flop Inputs	
S	A	В	g	A*	B*	J_{A}	K _A	S_B	R_{B}
0	0	0	0	1	0	1	X	0	X
0	0	1	1	0	1	Ó	X	X	
0	1	0	1	1	1	X	0	1	ă
0	1 %	1	0	0	0	X	1	Ó	
1	0 ,	0	0	1	0	1	X	Ó	×
1	0	1	1	1	1	1	X	X	
1	1	0	0	0	0	X	1	Ô	X
1	1	_1	0	1	0	×	Ó	0	1

- a) (4 Points) Fill in the missing values for the state table.
- b) (6 Points) Draw the state transition diagram based on the state table. State Diagram:



Problem 10)

(15 points) Design a Mealy state machine that will detect a 1010 sequence from an input s with overlap (e.g. the following stream of bits will cause the sequence to be detected twice: "101010".) Fill in the state table (the starting state is 00 and they are subsequently named in numeral order.) Make sure to use don't cares to fill in the implementation columns, when possible. Once you have the state table, calculate the next state logic for D1 and D0, and output logic for z using K-maps. Finally, draw the state machine circuit. Use D flip-flops for state memory. It may be useful to first construct a state transition diagram but only the state table will be graded. Note that the following page is available to you for additional workspace for this problem.

State Table

Present State		Input	Next State		Output	Flip Flop Inputs	
Q1	Q0	s	Q1*	Q0*	Z	D1	D0
0	0	0	0	٥	0	0	0
0	0	1	0	1	0	٥	1
0	1	0)	0	0	1	0
0	1	1	0	1	0	0	
1	0	0	0	0	0	0	0
1	0	1)	1	0		2
1	1	0	1	0		1	0
1	1	1	0		0	0	1

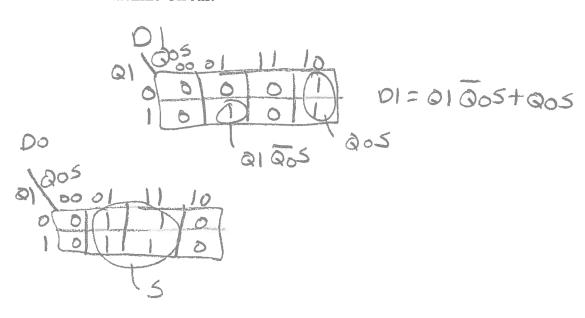
Next State Logic:

$$D1 = \frac{01005 + 005}{5}$$

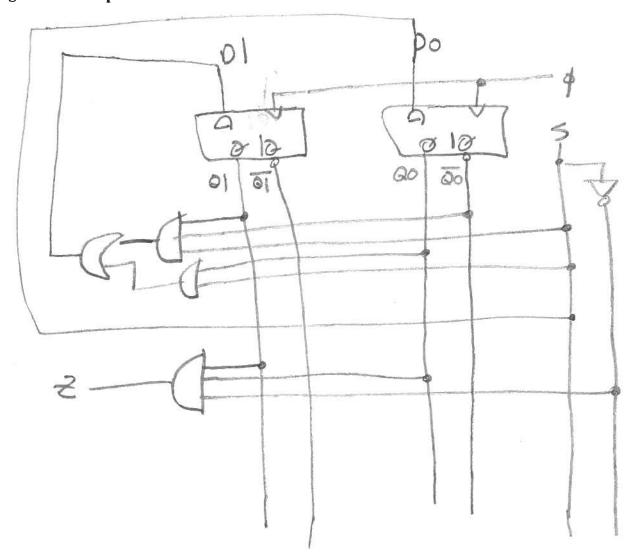
$$D0 = \frac{5}{5}$$

Output Logic:

State Machine Circuit



Blank page to use with problem 10.



(6 Points – 2 Points Each) In the circuit below, assume an initial value of 0 for Q. Complete the timing diagram for Q_a , Q_b and Q_c .

In the circuit below, assume an initial value of 0 for Q. Complete the timing diagram for Q_a , Q_b and Q_c .

