CPE 2211 COMPUTER ENGINEERING LAB

EXPERIMENT 5 LAB MANUAL

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HARDWARE VERIFICATION OF SEVEN SEGMENT DECODER

OBJECTIVES

In this experiment you will

- Gain experience with use of Karnaugh Maps.
- Gain practical experience with seven segment displays.
- Use the suite of EDA tools supplied by Altera: Quartus-II and ModelSim.
- Use the Altera FPGA DE2 Board verify in hardware with an FPGA.

LAB REPORTS

The format of lab reports should be such that the information can be used to reproduce the lab, including what values were used in a circuit, why the values were used, how the values were determined, and any results and observations made. This lab manual will be used as a guide for what calculations need to be made, what values need to be recorded, and various other questions. The lab report does not need to repeat everything from the manual verbatim, but it does need to include enough information for a 3rd party to be able to use the report to obtain the same observations and answers. Throughout the lab manual, in the Preliminary (if there is one), and in the Procedure, there are areas designated by **Qxx followed by a question or statement**. These areas will be **bold**, and the lab TA will be looking for an answer or image for each. These answers or images are to be included in the lab report. The lab TA will let you know if the lab report will be paper form, or if you will be able to submit electronically.

PURPOSE

The purpose of this exercise is to verify that the hardware realization of your seven segment decoder design performs as predicted by your logic simulation. You will use the seven segment decoder created in Lab 4 to program an Altera Cyclone II FPGA. You will need to make appropriate pin assignments so that inputs are mapped to the switches and the outputs are mapped to the different segments on one of the seven segment displays (see Appendix A).

Materials Required

Altera DE2 Board, Altera Cyclone II FPGA, Quartus II Software

PROCEDURE

1. Generate the configuration file. Refer to Lab 2 for detailed steps to complete this step.
2. There are 18 toggle switches [SW0 – SW17] on the DE2 board and are tied to specific pins

of the Cyclone II FPGA. These pin mappings are listed in Table A-1 of Appendix A. Assign the input ports [8,4,2,1] of your 7-segment design to appropriate switches on the DE2 board.

3. The DE2 board has eight 7-segment displays. The segments are active-low, applying a low logic level to a segment causes it to light up, and applying a high logic level turns it off. Configure the outputs of the 7-segment design [a – g] to appropriate segments [0 – 6] of the one of the seven segment displays. Output 'a' should be mapped to segment 0 and so on. The pin mapping for these segments is given in Table A-4 in Appendix A.
4. Once the pin mappings are completed, you are ready to configure the FPGA. Make sure the board is powered up and connected to the PC using the USB port.
5. Verify your circuit's logic function using the toggle switches and 7-segment display.

Q1. How many Logic Blocks does your design take (refer to Lab 3 for Logic Block specifics)?

Q2. How does that compare to the total number of primitive gates obtained in Lab 4.

Q3. How does that compare to the total number of primitive output gates you used (that is, the number of primitive gates that produced an output)?

Q4. What conclusions can you draw from this?

Q5. What is the worst case propagation delay of your circuit in nanoseconds? Estimates of this delay can be found in the .tan file in the project directory.

Q6. Which path (specified as input pin to output pin) has the worst case delay? This can be found in the .tan file in the project directory.