Appendix A
FPGA Board I/Os: Switches, LEDs, and 7-Segment Displays

Table A-1: Pin assignments for the toggle switches

Signal Name	FPGA Pin No.	Description
SW0	PIN_N25	Toggle Switch[0]
SW1	PIN_N26	Toggle Switch[1]
SW2	PIN_P25	Toggle Switch[2]
SW3	PIN_AE14	Toggle Switch[3]
SW4	PIN_AF14	Toggle Switch[4]
SW5	PIN_AD13	Toggle Switch[5]
SW6	PIN_AC13	Toggle Switch[6]
SW7	PIN_C13	Toggle Switch[7]
SW8	PIN_B13	Toggle Switch[8]
SW9	PIN_A13	Toggle Switch[9]
SW10	PIN_N1	Toggle Switch[10]
SW11	PIN_P1	Toggle Switch[11]
SW12	PIN_P2	Toggle Switch[12]
SW13	PIN_T7	Toggle Switch[13]
SW14	PIN_U3	Toggle Switch[14]
SW15	PIN_U4	Toggle Switch[15]
SW16	PIN_V1	Toggle Switch[16]
SW17	PIN_V2	Toggle Switch[17]

Table A-2: Pin assignments for the pushbutton (debounced) switches

Signal Name	FPGA Pin No.	Description
KEY0	PIN_G26	Pushbutton[0]
KEY1	PIN_N23	Pushbutton[1]
KEY2	PIN_P23	Pushbutton[2]
KEY3	PIN_W26	Pushbutton[3]

Table A-3: Pin assignments for the LEDs.

Signal Name	FPGA Pin No.	Description
LEDR0	PIN_AE23	LED Red[0]
LEDR1	PIN_AF23	LED Red[1]
LEDR2	PIN_AB21	LED Red[2]
LEDR3	PIN_AC22	LED Red[3]
LEDR4	PIN_AD22	LED Red[4]
LEDR5	PIN_AD23	LED Red[5]
LEDR6	PIN_AD21	LED Red[6]
LEDR7	PIN_AC21	LED Red[7]
LEDR8	PIN_AA14	LED Red[8]
LEDR9	PIN_Y13	LED Red[9]
LEDR10	PIN_AA13	LED Red[10]
LEDR11	PIN_AC14	LED Red[11]
LEDR12	PIN_AD15	LED Red[12]
LEDR13	PIN_AE15	LED Red[13]
LEDR14	PIN_AF13	LED Red[14]
LEDR15	PIN_AE13	LED Red[15]
LEDR16	PIN_AE12	LED Red[16]
LEDR17	PIN_AD12	LED Red[17]
LEDG0	PIN_AE22	LED Green[0]
LEDG1	PIN_AF22	LED Green[1]
LEDG2	PIN_W19	LED Green[2]
LEDG3	PIN_V18	LED Green[3]
LEDG4	PIN_U18	LED Green[4]
LEDG5	PIN_U17	LED Green[5]
LEDG6	PIN_AA20	LED Green[6]
LEDG7	PIN_Y18	LED Green[7]
LEDG8	PIN_Y12	LED Green[8]

Using the 7-segment Displays

The DE2 Board has eight 7-segment displays. These displays are arranged into two pairs and a group of four, with the intent of displaying numbers of various sizes. As indicated in the schematic in Figure A.1, the seven segments are connected to pins on the Cyclone II FPGA. Applying a low logic level to a segment causes it to light up, and applying a high logic level turns it off. Each segment in a display is identified by an index from 0 to 6, with the positions given in Figure A.2. Note that the dot in each display is unconnected and cannot be used. Table A-4 shows the assignments of FPGA pins to the 7-segment displays.

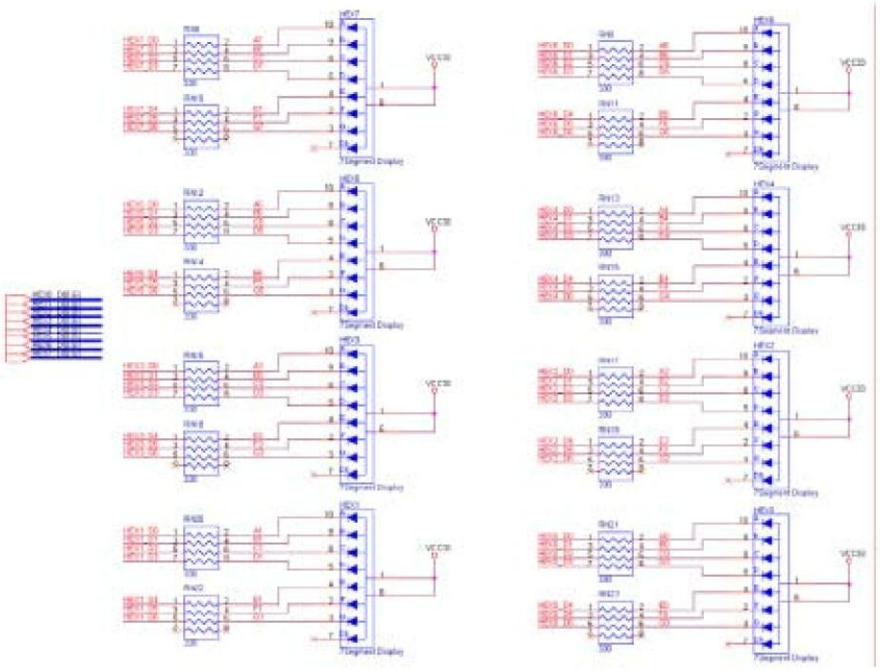

Figure A.1 Schematic diagram of the 7-segment displays.

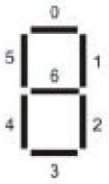

Figure A.2 Position and index of each segment in a 7-segment display.

Table A-4. Pin assignments for the 7-segment display.

Signal Name	FPGA Pin No.	Description
HEX0 0	PIN_AF10	Seven Segment Digit 0[0]
HEX0 1	PIN_AB12	Seven Segment Digit 0[1]
HEX0 2	PIN_AC12	Seven Segment Digit 0[2]
HEX0 3	PIN_AD11	Seven Segment Digit 0[3]
HEX0 4	PIN_AE11	Seven Segment Digit 0[4]
HEX0 5	PIN_V14	Seven Segment Digit 0[5]
HEX0 6	PIN_V13	Seven Segment Digit 0[6]
HEX1 0	PIN_V20	Seven Segment Digit 1[0]
HEX1 1	PIN_V21	Seven Segment Digit 1[1]
HEX1 2	PIN_W21	Seven Segment Digit 1[2]
HEX1 3	PIN_Y22	Seven Segment Digit 1[3]
HEX1 4	PIN_AA24	Seven Segment Digit 1[4]
HEX1 5	PIN_AA23	Seven Segment Digit 1[5]
HEX1 6	PIN_AB24	Seven Segment Digit 1[6]
HEX2 0	PIN_AB23	Seven Segment Digit 2[0]
HEX2 1	PIN_V22	Seven Segment Digit 2[1]
HEX2 2	PIN_AC25	Seven Segment Digit 2[2]
HEX2 3	PIN_AC26	Seven Segment Digit 2[3]
HEX2 4	PIN_AB26	Seven Segment Digit 2[4]
HEX2 5	PIN_AB25	Seven Segment Digit 2[5]
HEX2 6	PIN_Y24	Seven Segment Digit 2[6]
HEX3 0	PIN_Y23	Seven Segment Digit 3[0]
HEX3 1	PIN_AA25	Seven Segment Digit 3[1]
HEX3 2	PIN_AA26	Seven Segment Digit 3[2]
HEX3 3	PIN_Y26	Seven Segment Digit 3[3]
HEX3 4	PIN_Y25	Seven Segment Digit 3[4]
HEX3 5	PIN_U22	Seven Segment Digit 3[5]
HEX3 6	PIN_W24	Seven Segment Digit 3[6]
HEX4 0	PIN_U9	Seven Segment Digit 4[0]
HEX4 1	PIN_U1	Seven Segment Digit 4[1]
HEX4 2	PIN_U2	Seven Segment Digit 4[2]
HEX4 3	PIN_T4	Seven Segment Digit 4[3]
HEX4 4	PIN_R7	Seven Segment Digit 4[4]
HEX4 5	PIN_R6	Seven Segment Digit 4[5]
HEX4 6	PIN_T3	Seven Segment Digit 4[6]

HEX5 0	PIN_T2	Seven Segment Digit 5[0]
HEX5 1	PIN_P6	Seven Segment Digit 5[1]
HEX5 2	PIN_P7	Seven Segment Digit 5[2]
HEX5 3	PIN_T9	Seven Segment Digit 5[3]
HEX5 4	PIN_R5	Seven Segment Digit 5[4]
HEX5 5	PIN_R4	Seven Segment Digit 5[5]
HEX5 6	PIN_R3	Seven Segment Digit 5[6]
HEX6 0	PIN_R2	Seven Segment Digit 6[0]
HEX6 1	PIN_P4	Seven Segment Digit 6[1]
HEX6 2	PIN_P3	Seven Segment Digit 6[2]
HEX6 3	PIN_M2	Seven Segment Digit 6[3]
HEX6 4	PIN_M3	Seven Segment Digit 6[4]
HEX6 5	PIN_M5	Seven Segment Digit 6[5]
HEX6 6	PIN_M4	Seven Segment Digit 6[6]
HEX7 0	PIN_L3	Seven Segment Digit 7[0]
HEX7 1	PIN_L2	Seven Segment Digit 7[1]
HEX7 2	PIN_L9	Seven Segment Digit 7[2]
HEX7 3	PIN_L6	Seven Segment Digit 7[3]
HEX7 4	PIN_L7	Seven Segment Digit 7[4]
HEX7 5	PIN_P9	Seven Segment Digit 7[5]
HEX7 6	PIN_N9	Seven Segment Digit 7[6]

4.6 Using the Expansion Header

The DE2 Board provides two 40-pin expansion headers. Each header connects directly to 36 pins on the Cyclone II FPGA, and also provides DC +5V (VCC5), DC +3.3V (VCC33), and two GND pins. Figure 4.10 shows the related schematics. Each pin on the expansion headers is connected to two diodes and a resistor that provide protection from high and low voltages. The figure shows the protection circuitry for only four of the pins on each header, but this circuitry is included for all 72 data pins. Table A-5 gives the pin assignments.

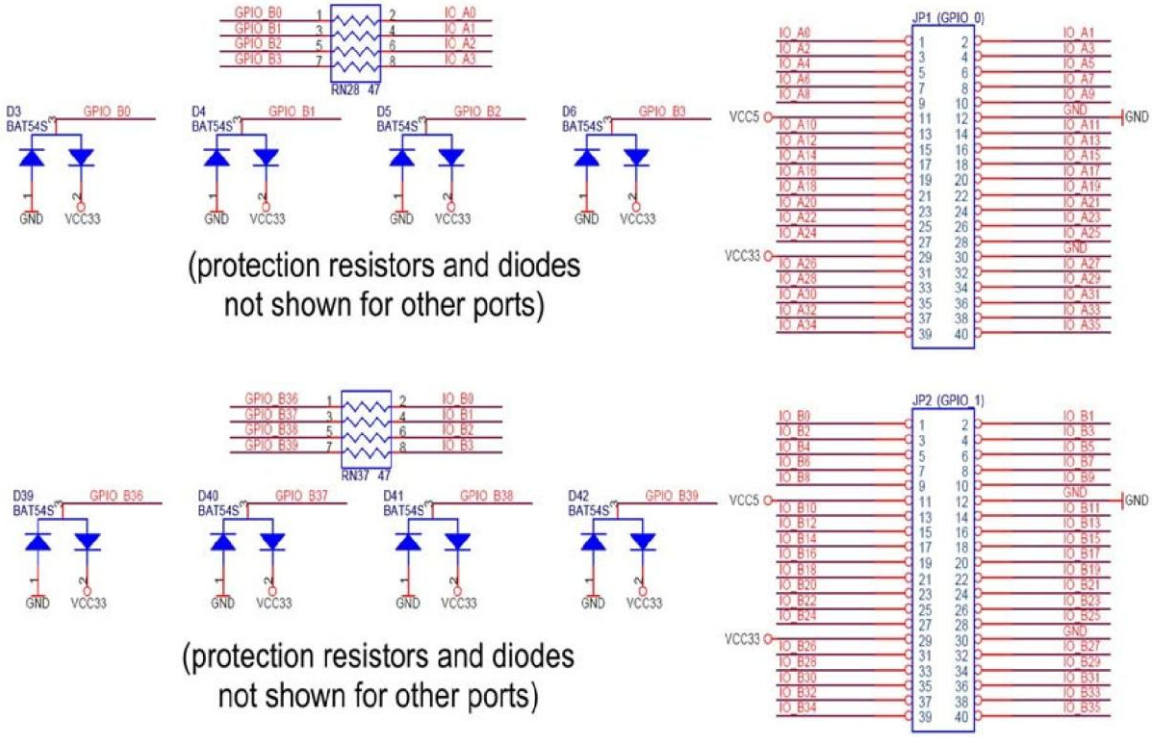

Figure 4.10. Schematic diagram of the expansion headers.

Table A-5: Pin assignments for expansion headers

Signal Name	FPGA Pin No.	Description
GPIO_0[0]	PIN_D25	GPIO Connection 0[0]
GPIO_0[1]	PIN_J22	GPIO Connection 0[1]
GPIO_0[2]	PIN_E26	GPIO Connection 0[2]
GPIO_0[3]	PIN_E25	GPIO Connection 0[3]
GPIO_0[4]	PIN_F24	GPIO Connection 0[4]
GPIO_0[5]	PIN_F23	GPIO Connection 0[5]
GPIO_0[6]	PIN_J21	GPIO Connection 0[6]
GPIO_0[7]	PIN_J20	GPIO Connection 0[7]
GPIO_0[8]	PIN_F25	GPIO Connection 0[8]
GPIO_0[9]	PIN_F26	GPIO Connection 0[9]
GPIO_0[10]	PIN_N18	GPIO Connection 0[10]
GPIO_0[11]	PIN_P18	GPIO Connection 0[11]
GPIO_0[12]	PIN_G23	GPIO Connection 0[12]
GPIO_0[13]	PIN_G24	GPIO Connection 0[13]
GPIO_0[14]	PIN_K22	GPIO Connection 0[14]
GPIO_0[15]	PIN_G25	GPIO Connection 0[15]
GPIO_0[16]	PIN_H23	GPIO Connection 0[16]
GPIO_0[17]	PIN_H24	GPIO Connection 0[17]
GPIO_0[18]	PIN_J23	GPIO Connection 0[18]
GPIO_0[19]	PIN_J24	GPIO Connection 0[19]
GPIO_0[20]	PIN_H25	GPIO Connection 0[20]
GPIO_0[21]	PIN_H26	GPIO Connection 0[21]
GPIO_0[22]	PIN_H19	GPIO Connection 0[22]
GPIO_0[23]	PIN_K18	GPIO Connection 0[23]
GPIO_0[24]	PIN_K19	GPIO Connection 0[24]
GPIO_0[25]	PIN_K21	GPIO Connection 0[25]
GPIO_0[26]	PIN_K23	GPIO Connection 0[26]
GPIO_0[27]	PIN_K24	GPIO Connection 0[27]
GPIO_0[28]	PIN_L21	GPIO Connection 0[28]
GPIO_0[29]	PIN_L20	GPIO Connection 0[29]
GPIO_0[30]	PIN_J25	GPIO Connection 0[30]
GPIO_0[31]	PIN_J26	GPIO Connection 0[31]
GPIO_0[32]	PIN_L23	GPIO Connection 0[32]
GPIO_0[33]	PIN_L24	GPIO Connection 0[33]
GPIO_0[34]	PIN_L25	GPIO Connection 0[34]
GPIO_0[35]	PIN_L19	GPIO Connection 0[35]
GPIO_1[0]	PIN_K25	GPIO Connection 1[0]
GPIO_1[1]	PIN_K26	GPIO Connection 1[1]
GPIO_1[2]	PIN_M22	GPIO Connection 1[2]
GPIO_1[3]	PIN_M23	GPIO Connection 1[3]
GPIO_1[4]	PIN_M19	GPIO Connection 1[4]
GPIO_1[5]	PIN_M20	GPIO Connection 1[5]
GPIO_1[6]	PIN_N20	GPIO Connection 1[6]
GPIO_1[7]	PIN_M21	GPIO Connection 1[7]
GPIO_1[8]	PIN_M24	GPIO Connection 1[8]
GPIO_1[9]	PIN_M25	GPIO Connection 1[9]
GPIO_1[10]	PIN_N24	GPIO Connection 1[10]
GPIO_1[11]	PIN_P24	GPIO Connection 1[11]
GPIO_1[12]	PIN_R25	GPIO Connection 1[12]
GPIO_1[13]	PIN_R24	GPIO Connection 1[13]
GPIO_1[14]	PIN_R20	GPIO Connection 1[14]
GPIO_1[15]	PIN_T22	GPIO Connection 1[15]
GPIO_1[16]	PIN_T23	GPIO Connection 1[16]
GPIO_1[17]	PIN_T24	GPIO Connection 1[17]
GPIO_1[18]	PIN_T25	GPIO Connection 1[18]

GPIO_1[19]	PIN_T18	GPIO Connection 1[19]
GPIO_1[20]	PIN_T21	GPIO Connection 1[20]
GPIO_1[21]	PIN_T20	GPIO Connection 1[21]
GPIO_1[22]	PIN_U26	GPIO Connection 1[22]
GPIO_1[23]	PIN_U25	GPIO Connection 1[23]
GPIO_1[24]	PIN_U23	GPIO Connection 1[24]
GPIO_1[25]	PIN_U24	GPIO Connection 1[25]
GPIO_1[26]	PIN_R19	GPIO Connection 1[26]
GPIO_1[27]	PIN_T19	GPIO Connection 1[27]
GPIO_1[28]	PIN_U20	GPIO Connection 1[28]
GPIO_1[29]	PIN_U21	GPIO Connection 1[29]
GPIO_1[30]	PIN_V26	GPIO Connection 1[30]
GPIO_1[31]	PIN_V25	GPIO Connection 1[31]
GPIO_1[32]	PIN_V24	GPIO Connection 1[32]
GPIO_1[33]	PIN_V23	GPIO Connection 1[33]
GPIO_1[34]	PIN_W25	GPIO Connection 1[34]
GPIO_1[35]	PIN_W23	GPIO Connection 1[35]

4.4 Clock Inputs

The DE2 board includes two oscillators that produce 27 MHz and 50 MHz clock signals. The board also includes an SMA connector which can be used to connect an external clock source to the board. The schematic of the clock circuitry is shown in Figure 4.8, and the associated pin assignments appear in Table 4.5.

Important: To use the 27 MHz clock, the TD_RESET pin (PIN_C4) must be asserted to a high logic level.

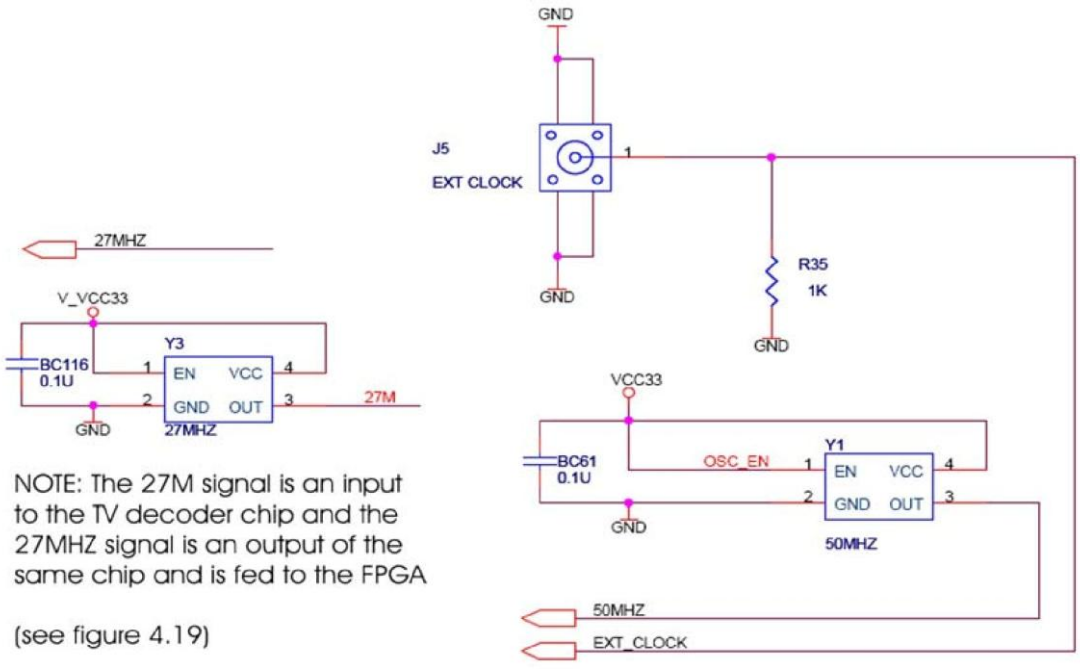

Figure 4.8. Schematic diagram of the clock circuit.

Table A-5: Pin assignments for clock inputs

Signal Name	FPGA Pin No.	Description
CLOCK_27	PIN_D13	27 MHz clock input
CLOCK_50	PIN_N2	50 MHz clock input
EXT_CLOCK	PIN_P26	External (SMA) clock input