EXPERIMENT NUMBER 13
SSI SEQUENTIAL LOGIC DESIGN: GENERAL SEQUENCE COUNTER

Purpose

The purpose of this exercise is to design, build, and document a simple sequence counter using the JK flip-flops.

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References

CpE112 Laboratory Manual: Appendix C, and Givone: Sections 4.4 – 4.6

Materials Required

Assorted SSI components including a 7476 dual Fip-Flop.

Preliminary

A simple sequence counter is shown in Figure 13-1. Design the counter shown in Figure 13-1 with the following steps:

1) Write a state transition table with the input (x), current state (Q_2Q_1), and next state ($Q_2^*Q_1^*$).
2) Find out the JK flip-flops corresponding to the transition table.
3) Write minimal logic expressions for $J_2, K_2 J_1, K_1$ using either a sum-of-products (SOP) or a product-of-sums (POS) (considering the unused states as don't care).
4) Draw a logic diagram for your SOP or POS expression.

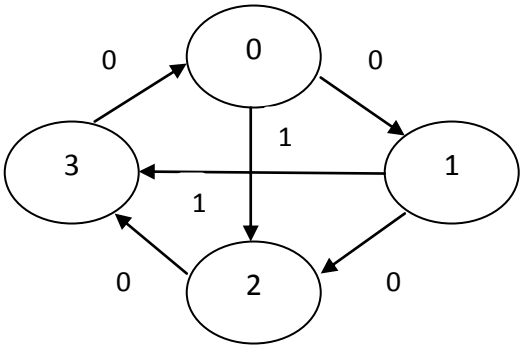

Figure 13-1.

Procedure

1) Build your design from the Preliminary using SSI components.
2) Test all state transitions for your design to verify that it behaves exactly as desired.