Answer the following questions:

(a) What is Computational Intelligence (CI)?

(b) Mention the paradigms (at least) of Computational Intelligence. With aid of a diagram, give examples of five hybrids with a brief explanation of each.
Answer the following questions:

(a) Describe three neuron models with aid of diagrams and equations.
(b) Describe briefly the commonly known types of neural network architectures today with aid of diagrams and give examples of each.
Problem: CM3  
Area: Computational Intelligence  
Code #__________

Answer the following questions:

(a) What is the difference between PSO and SPPSO? Provide the two advantages and disadvantages of these algorithms.

(b) Define the following terms:

(i) Neural network ensemble

(ii) Immunotronics
Answer the following questions:

(a) Define Swarm Intelligence (SI) and mention the five principles of SI.

(b) Describe the Ant Colony Optimization with equations.

(c) Describe the Particle Swarm Optimization with equations.
(d) Describe the properties of an artificial immune system (AIS) and provide three examples of AIS algorithms.
Problem: CM5  Area: Computer Architecture

Times taken by major hardware units in a MIPS processor are as follows:

- Memory read or write: 500ps
- Register file read and write: 200ps
- ALU operation: 400ps

a. What is the maximum clock frequency for a five-stage MIPS pipeline datapath?

b. Neglecting any hazards and resulting stalls, what are the pipeline latency and the cycles per instruction (CPI) for a long instruction sequence?

c. Compare this datapath with a single cycle datapath:

<table>
<thead>
<tr>
<th>Datapath</th>
<th>Clock cycle time</th>
<th>Clock frequency</th>
<th>CPI</th>
<th>Time per instruction</th>
<th>mips</th>
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<tbody>
<tr>
<td>Single-cycle</td>
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<td>Pipeline</td>
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Problem: CM6          Area: Computer Architecture          Code #_________

Answer the following questions:

(a) List the types of hazards in a pipeline datapath.

(b) Does the five stage MIPS pipeline execution of the following sequence of instructions generate any hazard? If yes, what type of hazard?

\[
\begin{align*}
\text{lw} & \quad t3, 0(s1) \\
\text{sub} & \quad s0, t0, t1 \\
\text{sub} & \quad t2, s0, t3
\end{align*}
\]

(c) If the instruction stream in (b) generates a hazard, could it be handled without a pipeline stall? Illustrate the handling of hazard by a sketch of pipeline stages.
Problem: CM7                Area: Computer Architecture                Code #__________

Answer the following questions:

(a) A one-level cache system is designed to speed up memory accesses of a processor. Suppose the data access from cache takes 1 clock cycle. The time to transfer data from the main memory to cache requires n cycles. How many clock cycles on an average will the processor take for accessing memory data?

(b) Suppose the CPI of a processor pipeline is 1 if there were no stalls. The access time for cache is 1 cycle and that for the main memory to cache is 10 cycles. What should be the hit rate of the cache if we want the average data access time not to exceed 1.5 cycles?

(c) Can we reduce the average data access time below 1.5 cycles obtained in (b) by making the cache faster with access time below 1 cycle and increase the processor throughput? If not, what are the possible ways to speed up the throughput? Give at least three ways.
IEEE 754 single precision floating point number format has one sign bit, 8-bit exponent, 23-bit significand and its exponent bias is 127 in decimal:

\[ (-1)^{\text{sign}} \times 1.\text{significand} \times 2^{\text{exponent} - 127} \]

(a) Find IEEE 754 single precision representations for \( A = -0.5 \) and \( B = +0.75 \) in decimal.

(b) Calculate \( A + B \) using floating point arithmetic.
Simplify the following Boolean expression using Boolean algebra:

\[ f(a,b,c) = ((a+bc+a'c)(a'+c'))' \]
Make an SR flip-flop out of the D flip-flop below. Show all your work and draw the resulting circuit.

<table>
<thead>
<tr>
<th>S</th>
<th>R</th>
<th>Qt</th>
<th>Qt+1</th>
<th>D</th>
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<tbody>
<tr>
<td>0</td>
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<td>0</td>
<td>0</td>
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\[
\begin{array}{cc}
D & Q \\
\end{array}
\]
Problem: CM11  Area: Integrated Circuits and Logic Design  Code #__________

Given the function $F(A,B,C,D)$ below (dc means don’t care). Answer the following questions.

$$F = \prod_{ABCD} M(0,5,7,9,10,13,15) + dc(1,4,12)$$

(a) Write the canonical POS expression for $F$.

(b) Determine the minimal POS expression for $F$.

(c) Draw the logic network for the minimal POS expression for $F$ found in part (b). You may use any combination of logic gates.
Answer the following questions below.

Convert 62 and −62 to 8-bit 2's complement representation.

Convert 41 and −41 to 8-bit 2's complement representation.

Perform the addition 62 + 41 in 8 bit 2's complement representation.

Perform the subtraction 62 - 41 in 8 bit 2's complement representation.

Perform the subtraction 41 - 62 in 8 bit 2's complement representation.
Problem: CM13  Area: Embedded Computer Systems  Code #________

Suppose that a microcontroller which has a 16-bit address port (from A0 to A15) controls three external memory devices: one 8K X 8 ROM (ROM1), one 1K X 8 ROM (ROM2) and one 8 bit register. The given microcontroller’s A15, A14 and A13 pins are used to select ROM1, ROM2 and register, respectively, and the other address pins (from A12 to A0) are used to address individual external memory device.

a) For each external memory device, find the address space (Remark: 16-bit starting address and 16-bit ending address must be shown for each device).

b) For the given ROM1 and ROM2, specify the used range of memory space and unused range of memory space (Remark: 16-bit starting address and 16-bit ending address must be shown).
ASM programming
(a) Write short sequences of ASM instructions which show how to use indirect addressing to (1) clear 25 memory locations starting with address 50H and (2) to access the 5th element of a lookup table which begins at address B2H.

(b) Write a short sequence of ASM instructions which will monitor the bit P1.2 continuously. When it is high, send 55H out P1.5 and when it is low send AAH out P1.7.
Three interrupts are active, T1 (the timer 1 interrupt), EX0 (external interrupt 0), and SER (the interrupt related to the serial port). The following diagram illustrates program execution as the interrupts come in. For example, the program begins executing "main", then jumps to the T1 interrupt service routine (ISR) when the T1 interrupt occurs, then to the serial ISR, etc. Assume there are two ISR priorities (low and high).

a. What is the priority of T1 (low or high)

b. What is the priority level of EX0 (low or high)

c. What is the priority level of SER (low or high)

d. For the last transition, where all three of the interrupts (T1, SER, and EX0) come in at the same time, which interrupt is executed first (i.e. which ISR is XX)? Assume their priorities have not changed over the course of execution. State any other assumptions you used to arrive at your conclusion or explain the conditions required to determine your answer.

e. Given the priority levels indicated in the figure above, what approximately is the MINIMUM and MAXIMUM time you expect between when the EX0 interrupt occurs and the ISR begins? State any assumptions you used to arrive at your conclusion.
Coding and Addressing
a. What is the difference between Assembler operation and Compiler operation? Explain.

b. What is the difference between Long Addressing and Absolute Addressing? How you decide to use either one of them if you are writing an 8051 assembly code?