Problem: CM1
Area: Computational Intelligence

Answer the questions for parts a-c below.

(a) What is Computational Intelligence (CI)?

(b) What is the different between the traditional Artificial Intelligence and the modern CI?

(c) Mention at least 5 paradigms of Computational Intelligence.
Problem: CM2
Area: Computational Intelligence

Answer the questions for parts a-c below.

(a) Are neural networks, as currently used in engineering, based on models of the human brain? Explain the reasons for your answer in detail.
(b) Given the following feedforward neural network in Fig. Q2 with a sigmoid function (given below) in the hidden layer and a linear function in the output layer

\[ d_j = \frac{j}{1 + e^{-a_j}} \]

**Fig. Q2**

Given that \([W_{11}, W_{12}, V_{11}, V_{12}] = [1.0, 0.5, -1, 0.5]\), calculate the output \(y\) for \(x = 0.5\).
(c) Recurrent neural networks and simultaneous recurrent networks are feedback neural networks. Explain the similarities and the differences between these networks.
Problem: CM3
Area: Computational Intelligence
Code #__________

Answer the questions for parts a and b below.

(a) Describe the different types of hardware evolution. Provide diagrams where possible.

(b) Define the following terms:

(i) Embryonics

(ii) Adaptive Devices, Circuits and Systems

(iii) Immunotronics
Answer the questions for parts a-c below.

(a) Define Swarm Intelligence (SI) and mention the five principles of SI.

(b) Briefly explain with the equations the difference between continuous PSO, binary PSO and integer PSO.
(c) Describe fuzzy system and its unique properties.
Find the minimal sum of products (SOP) and the minimal product of sums (POS) expressions for the minterm expression \( f(v,w,x,y,z) = \sum m(1,5,9,11,13,20,21,26,27,28,29,30,31) \).
Answer the questions for parts a and b below.

CMOS circuits.

a) For the CMOS circuit shown to the right, construct a function table in the style of the function tables in the text. Indicate whether each transistor is ON or OFF and the function output Z (H or L).

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Q1</th>
<th>Q2</th>
<th>Q3</th>
<th>Q4</th>
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<th>Q6</th>
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b) Determine the logic function for the logic CMOS circuit in part a.
Given the state table below with the state variables $X(t)$ and $Y(t)$, externally applied input $b(t)$ and output $g(t)$. Answer the questions for parts a and b below.

<table>
<thead>
<tr>
<th>Present Input</th>
<th>Present State</th>
<th>Present Output</th>
<th>Next State</th>
<th>JK Flip Flop Inputs</th>
<th>JK Flip Flop Inputs</th>
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</thead>
<tbody>
<tr>
<td>$b(t)$</td>
<td>$X(t)$</td>
<td>$Y(t)$</td>
<td>$g(t)$</td>
<td>$X(t+1)$</td>
<td>$Y(t+1)$</td>
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a) Fill in the missing values for the state table.

b) Draw the sequential circuit based on the state table.
Draw the 2-input NAND and 2-input NOR implementations for the logic expression $f(a,b,c) = \overline{abc} + \overline{a'bc'}$. 
A five-stage MIPS pipeline contains neither a forwarding unit nor a hazard resolution unit. Which part of the system should be responsible for correct execution of programs? Explain how. Show how a compiler would modify the following code so that it is correctly executed on this pipeline using fewest cycles:

```
sw $6, 0($7)  # Mem($7) ← $6
lw $8, 0($7)  # $8 ← Mem($7)
add $9, $8, $2 # $9 ← $8 + $2
```
The following is a series of address references given as word addresses:

1, 4, 8, 5, 20, 17, 19, 56, 9, 11, 4, 43, 5, 6, 9, 17

Assume that the system has a direct-mapped cache with 8 one-word blocks, and that the cache is initially empty. Label each reference in the above list as a hit or a miss and show the final contents of the cache. Because there are 8 words in the cache, an address x maps to the cache word location x modulo 8.
Identify all of the data dependencies in the following code. Which dependencies are data hazards that will be resolved via forwarding?

Add $2, $5, $4  // $2 = $5 + $4 and all operands are registers.
Add $4, $2, $5  // $4 = $2 + $5
Sw $5, 100($2)  // memory[$2 + 100] = $5
Add $3, $2, $4  // $3 = $2 + $4
Suppose we enhance a machine to make all floating-point instructions run four times faster. Let's look at how speedup behaves when we incorporate the faster floating-point hardware. If the execution time of some benchmark before the floating-point enhancement is 10 seconds, what will the speedup be if half of the 10 seconds is spent executing floating-point instructions?
Both timers and interrupts are used to set up RS-232 serial communications links on the 8051 microcontroller. Explain why both are necessary.
Embedded system programming is usually done in three different ways; 1) using assembly language, 2) using high level language such as C, or 3) combination of assembly and high level language. Discuss advantages and disadvantages of each programming option.
The schematic below shows several chips in external memory, including an alphanumeric LCD module. The "ENA" pin on the LCD module acts very much like the CE or CS chips on external memory modules, except that it operates with positive logic (i.e. the LCD module is selected when ENA is high). Note that for the 8051, both the low-address byte and data are sent through port P0, the high-address byte is sent out P2, RD/ and WR/ indicate when to read or write external data memory, ALE specifies when to read the low address byte, and PSEN/ indicates when to read code memory. The address bit numbers of the 8051 are indicated.

Answer the questions for parts a-c as follows.
Problem: CM15  Area: Embedded Computer Systems  Code #________

a) What is the address space of the LCD module?

b) Is the LCD module in code or data space? Explain your answer.

c) Could the AND gate be hooked to A15 and A13 instead of A15 and A14 (creating a different address space)? Why or why not?
Write a C-program which does the same as the following assembly code for the 8051 microcontroller. Assume instructions are written in the format:
<instruction> <destination>, <source>

mydata segment data
  x: DS 2 ; be sure to declare this variable in C program
  y: DS 1 ; be sure to declare this variable in C program

CSEG AT 0000H
  MOV x, #42D
  MOV A, #32D
  CLR C
  RLC A
  MOV R0,#0AH

LOOP:
  ADD A, R0
  DJNZ R0, LOOP
  MOV y, A
END
Answer the questions for parts a and b below.

(a) A US legislator proposed a law banning the deletion of any files from computer disks. This was to make forensic evidence easier to find. Fortunately, the proposal was not voted into law. From a security point of view (not a disk space perspective), describe a problem with this proposal if it had been passed.

(b) List four ways in which an attacker might obtain a victim’s password; you may use social engineering techniques as well as technological ones.
Answer the questions for parts a and b below.

(a) Explain what malware is and cite at least two publicized examples.

(b) Provide at least two countermeasures to detect and/or prevent malware disruptions.
Explain why all three of Mean Time Between Failure (MTBF), Mean Time to Repair (MTTR), and Mean Time to Failure (MTTF) are important in the reliability of a system.
Answer the questions for parts a and b below.

(a) Explain what a Denial of Service attack is.

(b) Explain how a DoS can be typically launched.
The traveling salesman problem is a known NP-Complete problem. You are given an n vertex weighted graph and the task is to find a cycle that includes all n vertices and has weight < k for some k. However, we may approximate a solution to it with a greedy approach.

Answer the questions for parts a-c below.

a. Construct a greedy algorithm to produce the minimum cost cycle for the traveling salesperson problem.

b. What is the running time complexity of your algorithm for the graph represented by (a) an adjacency list and (b) an adjacency matrix?

c. Show an example of your algorithm’s execution that shows it does not find the optimal solution.
The coin changing problem returns the minimal number of coins to make a total amount of change, \( C \). Argue that the greedy solution for the coin changing problem provides the optimal solution \( C = qQ + dD + nN + pP \), when \( q, d, n, \) and \( p \) are the number of quarters, dimes, nickels, and pennies, respectively, and \( Q, D, N, P \) are the values of Quarters, Dimes, Nickels, and Pennies (U.S. denominations).
The assignment problem is: Given \( n \) people and \( n \) jobs, where \( c(i,j) \) is the cost of assigning the \( i \)th person to the \( j \)th job, find an assignment of each person to a different job that minimizes the total cost of the job assignment. Thus, a sample problem looks as follows:

\[
\begin{bmatrix}
10 & 20 \\
11 & 100 & 200 \\
15 & 5 & 100
\end{bmatrix}
\]

\( n = 3, c = \)

Answer the questions for parts a-c below.

a. Provide a solution to this sample problem using the greedy method. Be clear in your choice of a greedy strategy.

b. Does the principle of optimality apply to this problem? Explain why or why not for full credit.

c. Solve the above sample problem using the choices made in applying the principle of optimality. You do not need to explicitly write down a recursion or tabular method, just show the steps.
Solve the following recurrence by assuming $n = 2^k$ for some non-negative integer, $k$:

$$\begin{align*}
T(n) &= 3T(n/2) + n & n > 4 \\
T(4) &= 14 & \text{otherwise}
\end{align*}$$

Verify your solution using mathematical induction (the substitution method).
A 12-bit Hamming code whose hexadecimal value is 0xE4F arrives at the receiver. Assume that one of the parity bits is in error.

(a) What is the 8-bit data value that was transmitted?
(b) What was the correct Hamming code (original) value in hexadecimal?
A TCP machine is sending full windows of 65,535 bytes over a 1 Gbps channel that has a 10 msec one-way delay. What is the maximum throughput achievable? What is the line efficiency?
Answer the questions in parts a and b below.

(a) List the two major classes or types of network routing algorithms and give an example of each type.

<table>
<thead>
<tr>
<th>Type/Class</th>
<th>Example</th>
</tr>
</thead>
<tbody>
<tr>
<td>(i)</td>
<td></td>
</tr>
</tbody>
</table>

(ii) 

(b) Random routing is defined as follows:
Upon receipt of an incoming packet to re-transmit, a node selects only one out-going path at random, excluding the link on which the packet arrived.

(i) Cite one advantage of random routing.

(ii) Cite one disadvantage of random routing.

(iii) What type of routing is random routing according to your classification scheme in part a?
Answer the questions for parts a, b, and c below.

(a) Compare the delay in sending an \( x \)-bit message over a \( k \)-hop path in a circuit-switched network and in a (lightly loaded) packet-switched network. The circuit setup time is \( s \) sec, the propagation delay is \( d \) sec per hop, the packet size is \( p \) bits, and the data rate is \( b \) bps. A justification is expected for every component of the delay.

(b) Assume that the setup of the circuit-switched network is carried out by the exchange of very short (much less than \( x \) bits) messages. Express the setup time, \( s \), in terms of the other network parameters provided in part a.

(c) Under what conditions does the packet network have a lower delay?