Computer Engineering 2211: Computer Engineering Laboratory
Prior Number – Computer Engineering 112

Credit and Contact Hours
1 credit hour laboratory (One 1-hour and 50-minute laboratory per week). Computer Engineering 2211 (112) is a laboratory complement to Computer Engineering 2210 (111), taken simultaneously or after Computer Engineering 2210 (111).

Instructor
Graduate Teaching Assistants coordinated by a faculty member
Faculty Coordinator Varies – J. Stanley, Ph.D.; J. Seiffertt, Ph.D.; M. Choi, Ph.D.

Text(s)
Available at:  http://ece.mst.edu/currentcourses/classnotesinfo/


Catalog Description
Introduction to digital design techniques, logic gates, Medium Scale Integration (MSI) parts and flip-flops, Timing analysis, Programming and use of Programmable Logic Devices (PLDs).

Prerequisite
Preceded or accompanied by Computer Engineering 2210 (111).

Required or Elective
Required

Course Goals
General Outcomes
1. Develop and simulate digital logic circuits using industrial-strength CAD tools such as Quartus.
2. Test digital hardware using discrete logic components, FPGAs, and typical laboratory equipment, e.g., logic analyzer/oscilloscope, function generator.
3. Demonstrate fundamental understanding of logic design and analysis, number systems, memory elements, timing, and elements of microprocessor organization through development and execution of laboratory experiments.
4. Document technical and experimental material for archival purposes or for knowledge transfer.
Relationship of Course to Program Outcomes

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S – strong connection; M – medium connection; W – weak connection

Topics Covered
1. Introduction to lab safety, laboratory equipment, and email (1 week)
2. Use of an Oscilloscope, Function Generator, Programmable Power Supply, and Counter, as applied to digital circuits (1 week)
3. Introduction to digital design with Quartus tools, schematic capture and logic simulation, and design of a two-input logic circuit using discrete gates (1 week)
4. Introduction to Altera FPGAs and Altera FPGA DE board. (1 week)
5. Design of a multifunctional gate using discrete components. (1 week)
6. Introduction to more advanced features of Schematic Capture and Simulation using Quartus. Hierarchical design, schematic capture and simulation of a Full Adder. (1 week)
7. Design, schematic capture, and simulation of a 7-segment decoder (1 week)
8. Design, testing, and verification of the 7-segment decoder with Xilinx (1 week)
9. Introduction to VHDL, vcom, and vsim. Design of a multi-function gate through modification of existing VHDL code (1 week)
10. Use of RAM/ROM to implement combinational logic. Further exploration of discrete components/testing (1 week)
11. Design, simulation, and hardware verification of a Registered ALU (2 weeks)
12. Design and implementation of a generalized sequence counter (1 week)
13. Design and simulation of a Control Unit (1 week)
14. A lab practical over the students’ proficiency in the use of laboratory software and equipment, and other material covered (1 week)