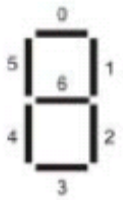
Appendix B

Binary to Seven Segment Decoder

In- order to utilize the seven segment displays of the Altera DE-2 FPGA board it is important that a generalized module of a seven segment decoder be made.

A Seven Segment Decoder takes in 4 inputs and has 7 outputs corresponding to the 7 segment display. The following figure shows the 7 segment display.

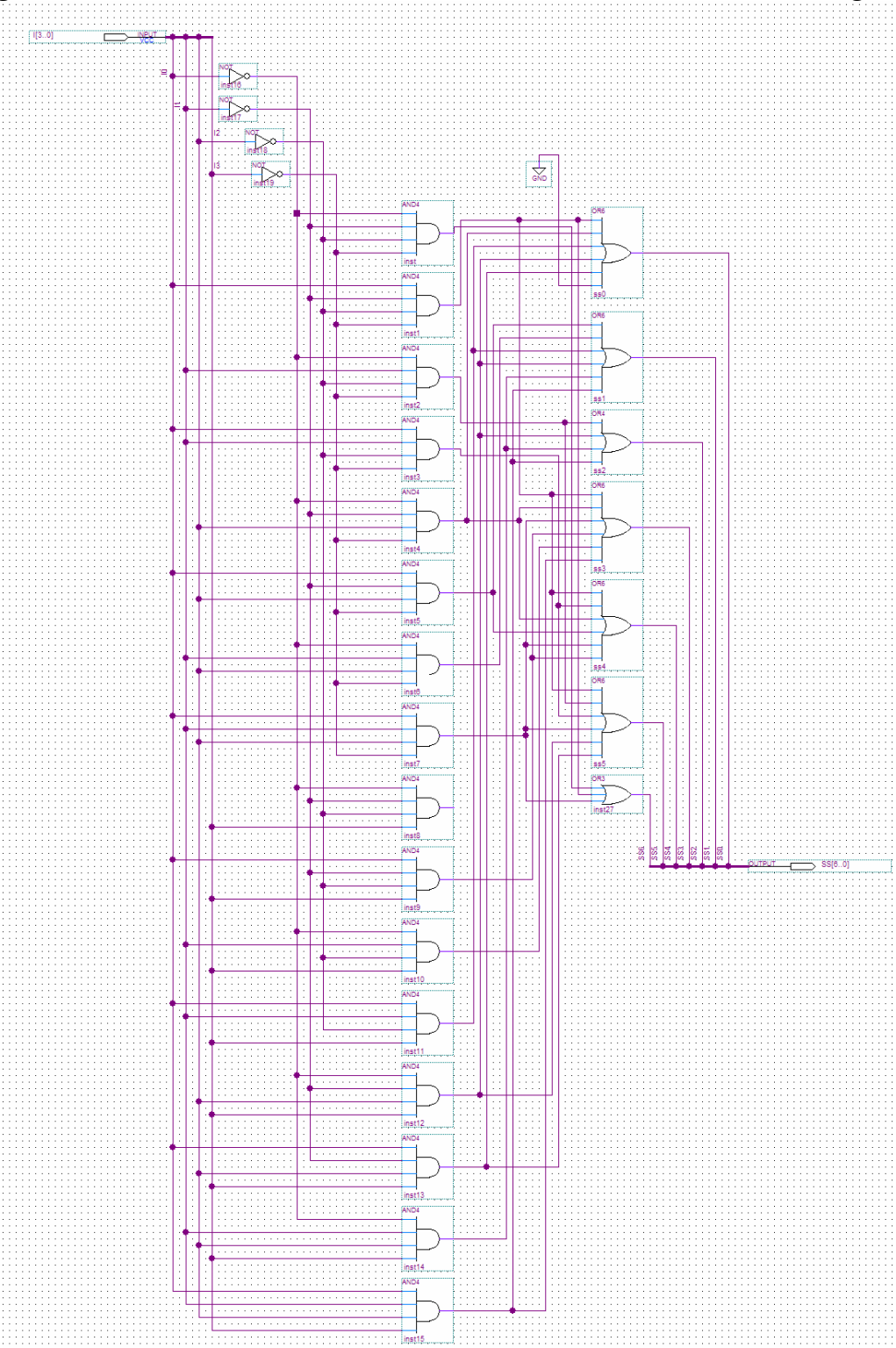


The truth table that is required for the conversion of the input binary stream into the 7 segment outputs has been given below.

Digit	A	B	C	D		0	1	2	3	4	5	6
0	0	0	0	0		0	0	0	0	0	0	1
1	0	0	0	1		1	0	0	1	1	1	1
2	0	0	1	0		0	0	1	0	0	1	0
3	0	0	1	1		0	0	0	0	1	1	0
4	0	1	0	0		1	0	0	1	1	0	0
5	0	1	0	1		0	1	0	0	1	0	0
6	0	1	1	0		0	1	0	0	0	0	0
7	0	1	1	1		0	0	0	1	1	1	1
8	1	0	0	0		0	0	0	0	0	0	0
9	1	0	0	1		0	0	0	1	1	0	0
10	1	0	1	0		0	0	0	1	0	0	0
11	1	0	1	1		1	1	0	0	0	0	0
12	1	1	0	0		0	1	1	0	0	0	1
13	1	1	0	1		1	0	0	0	0	1	0
14	1	1	1	0		0	1	1	0	0	0	0
15	1	1	1	1		0	1	1	1	0	0	0

Above truth table implies for driving the seven segment display.

Now depending upon the truth table, using and gates, not gates and other basic logic gates, a schematic can be made in the Quartus-II software as shown in the figure below.



Now assign the pins to the input and the output and compile the design and convert it to a symbol so that the symbol can be used in the future modules as well.