EXPERIMENT NUMBER 5
HARDWARE VERIFICATION OF SEVEN SEGMENT DECODER

Purpose

The purpose of this exercise is to verify that the hardware realization of your seven segment decoder design performs as predicted by your logic simulation. You will use the seven segment decoder created in an earlier exercise to program an Altera Cyclone II FPGA. You will need to make appropriate pin assignments so that inputs are mapped to the switches and the outputs are mapped to the different segments on one of the seven segment displays (see Appendix A).

References

None

Materials Required

Altera DE2 Board, Altera Cyclone II FPGA, Quartus II Software

Procedure

1. Generate the configuration file. Refer to Lab 4 for detailed steps to complete this step.
2. There are 18 toggle switches [SW0 – SW17] on the DE2 board and are tied to specific pins of the Cyclone II FPGA. These pin mappings are listed in Table A-1 of Appendix A. Assign the input ports [8,4,2,1] of your 7seg design to appropriate switches on the DE2 board.
3. The DE2 board has eight 7-segment displays. The segments are active-low, applying a low logic level to a segment causes it to light up, and applying a high logic level turns it off. Configure the outputs of the 7seg design [a – g] to appropriate segments [0 – 6] of the one of the seven segment displays. Output "a" should be mapped to segment 0 and so on. The pin mapping for these segments is given in Table A-4 in Appendix A.
4. Once the pin mappings are completed, you are ready to configure the FPGA. Make sure the board is powered up and connected to the PC using the USB port.
5. Verify your circuit's logic function using the toggle switches and 7-segment display.

Questions

1. How many configurable logic blocks does your design take?
2. How does that compare to the total number of primitive gates obtained in lab 5.
3. How does that compare to the total number of primitive output gates you used (that is, the number of primitive gates that produced an output)?
4. What conclusions can you draw from this?
5. What is the worst case propagation delay of your circuit in nanoseconds? Estimates of this delay can be found in the .tan file in the project directory.
6. Which path (specified as input pin to output pin) has the worst case delay? This can be found in the .tan file in the project directory.