# EXPERIMENT NUMBER 12
# GENERAL SEQUENCE COUNTER

**Purpose**

The purpose of this exercise is to design and build a general sequence counter

**References**

Givone: Sections 7.1 – 7.3

**Materials Required**

Quartus II, ModelSim

**Discussion**

A general sequence counter is to be designed such that it counts in a clockwise fixed loop when input X is 1, and in a counterclockwise loop, skipping every other state, when X is 0, as shown in Figure 12-1. The output of your state machine should be its count. The specific count for each state will be given to you by your instructor. You should write the assigned count for each state in the state diagram of Figure 12-1.

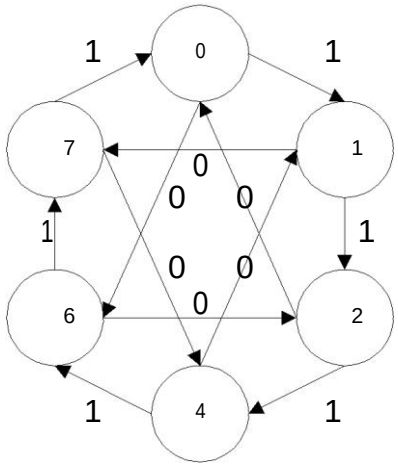


**Figure 12-1:** State Diagram of the General Sequence Counter

**Procedure**

1) Design the counter shown in Figure 12-1, using as few logic levels as possible. Any person using the minimal number of logic levels will receive 10% extra credit for this lab. Include the following to document your design:
   - state transition table
   - next state equations
   - schematic diagram
   - state diagram including unused states
2) Simulate your design using ModelSim. Print out the logic diagram, and the waveforms for all possible state transitions.

**Questions**

1) What are some typical applications of general sequence counters?
2) What factors determine the maximum clock frequency?