The viability of cache systems depends on the concept of locality.

1. Explain how a loop structure in a program exhibits both temporal and spatial locality.

2. Suppose we have three arrays x, y, and z stored contiguously in memory (that is, the y array starts at the memory location where the x array ends, etc.)

Describe how to access the three arrays in a way that maximizes the benefits of a cache.

Describe how to access the three arrays in a way that minimizes the benefits of a cache.
Suppose we enhance a computer to make all floating-point instructions run five times faster. Plot the speedup obtained, versus the fraction of time in the original computer spent during floating-point operations, on a graph given below. Make sure to show your calculations.
When adding two n-bit signed (2’s complement) binary numbers A and B, the following Boolean expression can be used to detect overflow where \( a_i \) and \( b_i \) are bits at bit position \( i \) in A and B, and \( s_i \) is the sum bit at bit position \( i \):

\[
OV = a_{n-1} \cdot b_{n-1} \cdot s_{n-1} + a_{n-1} \cdot b_{n-1} \cdot s_{n-1}
\]

A simpler formula for overflow detection is given as:

\[
OV = c_n \oplus c_{n-1}
\]

where \( c_{n-1} \) and \( c_n \) are the carry-in and carry-out of the leftmost full adder.

Prove that this simpler formula is equivalent to the previously given formula by showing the following two cases are equivalent to two product terms in the previously given formula:

**Case 1: 0 carried in, and 1 carried out.**

**Case 2: 1 carried in, and 0 carried out.**
Consider the dynamic branch predictor given below. Calculate the branch prediction accuracy ratio (= total number of correct branch predictions / total number of branch trials) for the following branching pattern: T-T-T-N-N-T-N-T-N-N-T-T-T, where T means a branch actually taken and N means a branch actually not taken. Assume that the starting state is one at the top-left corner.
Find the minimal sum and the minimal products expressions for the function
\[ f(v, w, x, y, z) = \prod M(0, 13, 15, 16, 17, 18, 19, 20, 21, 23, 27, 31). \]
Size the following complex gate so that it has the worst-case drive strength of an equivalent inverter with \(PW = 3\) and \(NW = 2\).
Answer the questions for parts a and b below.

a) Define latch and flip-flop as memory devices, including different types of implementations and physical operation based on the clock or input signal. Provide two examples of real-world devices that use latches and two examples of real-world devices that use flip-flops.

b) Describe the difference between a rising edge and a falling edge flip-flop. Illustrate the difference using a schematic/drawing.
Draw the transistor-level circuit for the layout shown below.
Answer all three questions below.

a. In the context of computer networks, describe the difference between error-detecting and error-correcting codes.

b. Describe why networks might use an error-correcting code instead of error detection and retransmission.

c. Give two applications where error-correcting codes are used and two applications where error detection and retransmission are used.
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Answer both questions below.

a. Describe the operation/purpose of each layer (physical, data link, network, transport, session, presentation, application) of the ISO OSI (Open Systems Interconnection) model.

b. Why do the different layers exist in this model?
Answer all four questions below.

a. Consider a half-duplex point-to-point link using a stop-and-wait scheme, in which a series of messages is sent, with each message segmented into a number of frames. Ignore errors and frame overhead. What is the effect on line utilization of increasing the number of frames for a constant message size? Justify your answer.

b. Why is pulse code modulation preferable to delta modulation for encoding analog signals that represent digital data? Note that such signals have high-frequency components and hence change rapidly.

c. What key factors affect channel capacity? Justify your answer using the Shannon theorem.

d. What geometric shape is used in cellular system design? Why?
Answer both questions below.

a. What percentage of the total IP address space does each of network classes A through C represent? Justify each answer.

b. Given a company with five individual departments, each department of which has eleven computers or networked devices, what mask (expressed in binary) could be applied to the company network to provide the subnetting necessary to divide up the network equally?