**General Information for CpE Qualifying Exam**

The Computer Engineering Qualifying exam is divided into a morning session and an afternoon session. Each session is of three hour duration. There are several options available for both the morning and afternoon exam, as detailed below. Before registering for the exam, the student should discuss these options with their PhD advisor. While the student may propose their exam choices to their PhD advisor, all choices are subject to the advisor’s final approval.

**Morning Session**

The morning session problems are selected to cover fundamental material in Computer Engineering in order to demonstrate breadth of knowledge in the field. Each student will answer questions from four of the seven selected emphasis areas. The emphasis areas in Computer Engineering are:

1. Computers and Architecture
2. Integrated Circuits and Logic Design
3. Embedded Computer Systems
4. Computational Intelligence
5. Networking
6. Security and Reliability
7. Electrical Engineering, with sub-areas:
   a) Power
   b) Communications / Signal Processing
   c) Controls
   d) Electromagnetics
   e) Circuits / Electronics
8. Computer Science, with sub-areas:
   a) Data Structures
   b) Algorithms

If Electrical Engineering is one of the areas chosen, then a sub-area of EE must also be identified.

As a general rule, basic material from undergraduate and 5xxx-level courses will be covered in the morning session although some material, of a fundamental nature, may be from 6xxx-level courses. The problems are designed so that each problem should take approximately 10-15 minutes to work. The student is required to work three out of the four questions in each of the four selected areas (12 questions total).

**Afternoon Session**

The afternoon session is designed to be more in-depth in order to demonstrate proficiency in specific areas of Computer Engineering. Three options for the afternoon session are available as follows:
Option 1  The student and advisor select a primary emphasis area from CpE Emphasis Areas 1-6 when registering for the exam. A secondary emphasis area is also chosen from CpE Emphasis Areas 1-7, excluding the selected primary emphasis area. If EE is chosen as a secondary emphasis area, then a sub-area of EE must also be chosen. During the exam, the student will be asked to answer four out of the five questions in the selected primary area and two out of the five questions in the secondary area (if EE is chosen then the student will answer two out of the four questions in the secondary area).

Option 2  The advisor and two other S&T graduate faculty members will jointly give an oral exam for 1-3 hours. The content of and requirements for this oral exam will be determined by these faculty members.

Option 3  The student may be exempted from a portion of the afternoon exam through proven scholarly work consisting of one of the following (assuming first or primary author):
   a)  Accepted / funded proposal in excess of $10,000
   b)  Accepted / published journal paper
   c)  Submitted journal paper
All submissions must be reviewed and approved by the advisor and CpE Associate Chair. Only the highest quality proposals or articles in well-respected journal, such as those published by IEEE, ACM, or Elsevier, will be approved. The advisor and CpE Assistant Chair will determine the portion(s) of the afternoon exam which the student will have to take, if any.

Reference Material

No reference material is allowed. The only items students are allowed to bring to the exam are pencils, pens, erasers, and calculators. Extra answer sheets will be provided by the exam proctor upon request. Extra calculator batteries or other supplies will not be available from the exam proctor. In order to keep track of the amount of time remaining during the exam each student should bring his or her own watch.

Grading for PhD Exam

Each problem on the CpE exams will be graded by the faculty member who wrote the problem. The student’s score is determined in two ways, as detailed below. The student passes the exam if their score is greater than 80% using either of the two methods:
   o  Questions are graded on a scale from 0-100%. The average score is determined for both the morning and the afternoon session. The student passes the exam (morning or afternoon) if they receive an average score greater than or equal to 80%.
   o  Each question is scored as pass/fail. The student passes a question if their score is 80% or higher. A student passes the morning or afternoon session if they pass 80% or more of the questions. For example, a student will pass the morning session if they score 80% or better on 10 of the 12 questions answered.
Students must pass both the morning and afternoon session to pass the qualifying exam.
Students who fail the PhD Exam on their first attempt will be given a second opportunity to pass the exam when it is given in the following semester. Students who fail the morning or afternoon exam but not both, need only to retake the exam failed. The student, with the advisor’s approval, may choose a different exam format if they wish (for example, the student may select different emphasis areas). Students who fail the exam once and do not take the exam in the subsequent semester will no longer be considered PhD candidates in this department.

A candidate who fails the CpE PhD Qualifying Exam on two consecutive tries may file a written petition with the ECE Graduate Studies Committee for a third attempt. The ECE Graduate Studies Committee will vote, by simple majority, to approve or deny the petition. If the petition is approved, it will be forwarded to the Office of Graduate Studies as a request to waive the requirement for passing the PhD Qualifying Exam by the end of the second semester after completion of the M.S. degree.

**Additional Information**

The following material, broken down by area, is intended to provide you with more information on the exam. Previous PhD Qualifying Exam problems are now posted on the department web site at [http://ece.mst.edu/usefullinks/qualifyingexams.html](http://ece.mst.edu/usefullinks/qualifyingexams.html).

1. **Computers and Architecture**

Topics covered in this exam are covered primarily in CpE 5110, CpE 5120, and CpE 6110 (afternoon session only) and include the following:

**Morning session topics**

1. Performance measurement and benchmarking
   - Throughput and delay
   - SPEC benchmarks
2. Principles of instruction set design
   - Computer hardware operations
   - Instruction set architecture
3. Pipelining, pipeline hazards and precise exceptions
   - Basics of pipelining and performance enhancement
   - Pipelined datapath
   - Pipelined control
   - Data and branch hazards
4. Caches, measuring cache performance, and methods for enhancing cache performance
   - Basics of Caches and performance enhancement
   - Cache performance analysis
   - Memory hierarchy
5. Dynamically scheduled pipelines
   - Thornton's scoreboard
   - Tomasulo's algorithm
   - Re-order buffer
6. Branch prediction
   • Basics of branch prediction
   • Branch-prediction buffers
   • Branch-target buffers
7. Virtual memory and virtually indexed caches
   • Basics of virtual memory
   • Process protection

Afternoon session topics

1. All morning session topics
2. Speculative execution
   • Combining dynamic scheduling, branch prediction and superscalar execution
3. Multiple issue microprocessors
   • Instruction level parallelism with multiple issue
   • Superscalar execution
   • Multiple instruction issue with dynamic scheduling
   • Very long instruction word (VLIW) approach
4. Multiprocessor cache coherence and snoopy caches
   • Centralized shared-memory architectures
   • Distributed shared-memory architectures
   • Coherence protocols

Recommended reference:

2. Integrated Circuits and Logic Design

Topics covered in this exam are covered primarily in CpE 2210, CpE 5210, and CpE 5220 and include the following. Items marked with afterwards (general knowledge) indicates that only general knowledge of the topic is required.

Morning Section Topics:
1) Numbering system conversions (B ↔ D, B ↔ H, H ↔ D)
2) logical operators (AND, OR, XOR, etc.)
3) Boolean Algebra
4) Truth Tables, SOP, POS, Minterm, Maxterm, and canonical form
5) K-maps (up to 6 variables)
6) design of an arbitrary function using static CMOS complementary logic (with and without an output inverter)
7) digital components (mux, demux, decoder, half-adder, full-adder, etc.)
8) area, speed, and power tradeoffs
9) 2^8 complement, sign magnitude, and unsigned formats (addition, subtraction, multiplication, division)
10) complete logic sets
11) flip-flops and registers
12) logic arrays
13) Binary Coded Decimal (BCD)
14) calculating circuit delay parameters, given component delay information (e.g., calculate minimum clock period given component propagation delays and flip-flop setup and hold times)
15) mux for implementing an arbitrary function
16) constructing larger mux/demux from smaller ones
17) adder circuits (RCA, CLA, CSA)
18) SRAM
19) IEEE floating-point numbers (addition, subtraction, multiplication, division)
20) fixed-point fractional numbers and round-off error
21) Mealy and Moore state machines
   - state table
   - state diagram
   - logic diagram
   - state minimization
   - Armstrong-Humphrey rules for binary state assignment
   - resetting vs. non-resetting sequence detectors
22) VHDL
   - entity and architecture statements
   - behavioral, structural, and dataflow models (for both combinational and synchronous circuits)
   - testbenches

Afternoon Section Topics:
1) All Morning Section Topics
2) VHDL
   - packages, functions, procedures, types, constants
   - generic constants and components
   - generate statements
   - file I/O
3) Algorithmic State Machines (ASMs)
   - timing chart
   - datapath
   - throughput capability (TPC)
   - demand driven handshaking convention
4) VLSI Design levels of abstraction:
   - Behavioral
   - Structural
   - Physical
5) CMOS Transistor Technology
   - Physical structures of nMOS and pMOS Enhancement Transistors
   - MOS Device Design Equations
     + Threshold voltage
     + Body Effect
- Analysis of MOS Inverters
  + DC Characteristics
  + Switching Threshold
  + Power, Energy and Delay
  + Noise Margin
  + Capacitance computation
  + Scaling CMOS inverters
- Static Load MOS Inverters

6) Circuit Characterization and Performance Estimation
- MOS Transistors Models
  + SPICE models
- Switching Characteristics
  + Analytical Delay Models
    Fall time, Rise time and Delay time
    Empirical delay models
    Gate delays
- Interconnect Parameters Estimation:
  + Capacitance
    Routing capacitance
    Diffusion capacitance
    Capacitance design guide
  + Resistance
  + Inductance  (general knowledge)
- The Wire Models:
  + The lumped models
  + The lumped RC models
  + Wire length design guide
- CMOS Primitive gate design
  + NAND, NOR, MUXs, Decoders, Encoders, Buffers, Inverters

7) CMOS Circuit Design:
- CMOS logic gate design
  + Optimization of CMOS circuit
  + Transistor sizing
  + Fan-in and Fan-out
  + Scaling of MOS transistors dimensions
- Power Dissipation
- CMOS Logic Structures
  + Static CMOS Complementary Logic
  + Dynamic CMOS Logic
    Charge sharing
    CMOS domino logic
  + Pass transistor logic

8) Static Timing Analysis and Clocking
- System timing
- Setup and Hold time
  + Latches and Flip-flops
- Synchronous timing issues
  + Single-phase clock design
  + Multi-phase clock design
- Clock Distribution Design
  + PLL and DLL (general knowledge)
  + Skew and Jitter (general knowledge)

9) Systems Design
- Packaging, Placement and Routing
- CMOS memories and Arrays (general knowledge)
  + Read-Write Memories (RAM)
  + Read Only Memories (ROM)
  + Programmable Logic Arrays (PLA)
  + Memory Peripheral Circuitry
- I/O Structures (general knowledge)

Recommended references:
- Digital Integrated Circuits, A design Perspective; Rabaey et.al.
- Principles of CMOS VLSI Design, A System Perspective, Weste and Eshraghian
- Modern VLSI Design, Wolf

3. Embedded Computer Systems


The morning exam focuses on the most fundamental topics in embedded systems, which are primarily covered in CpE 3150. Topics include:

- **Interpret and design hardware and software for simple real-time digital systems.**
  - Describe the fundamentals of microprocessor organization and operation. Show the transfer of information, from register to register or from register to memory, that occurs within a simple, generic processor for each instruction within its instruction set. Modify processor to perform new functions.
  - Describe the basis for interaction between a microcontroller and external hardware. Interpret and design digital system incorporating a microcontroller and common peripherals (RAM, ROM, A/D converters, etc). Explain the operation of timers, counters, and interrupts.
  - Write programs in C or ASM for a simple microcontroller.
• Write programs using interrupts to: perform a task at regular intervals using counters; to communicate between processors serially; or to provide immediate service to external hardware. Describe and build a task scheduler. Describe the basis behind existing real-time operating systems (RTOS) and implement simple programs with these systems.

• Recommended references:
  • CpE 3150 course web page: [http://web.umr.edu/~daryl/classes/ee213/](http://web.umr.edu/~daryl/classes/ee213/).

The afternoon exam will include more advanced questions from CpE 3150 and will also include questions from material covered in CpE 5151 and CpE 5170.

Topics related to CpE 5151 (Digital Systems Design Lab) include:
• Design the interface for microprocessor peripherals and create the timing diagrams for that interface.
• Describe the metastable state, what causes it and how to prevent it.
• Describe different types of programmable logic devices and write a PLD design program.
• Describe different types of logic families and the problems that can occur when using high speed digital logic signals such as transmission line effects and noise propagation.

Topics related to CpE 5170 (Real Time Systems) include:
• Hard vs Soft Real Time (R-T) Systems and Life-Cycle Models
• Specifications Model & Architecture Model
• Reference Model
• Multi-Tasking and R-T Scheduling
• Clock-Driven Scheduling
• Priority-Driven Scheduling
• Resource and Access Control
• Recommended references:

4. Computational Intelligence

The morning session covers all 5xxx level course materials and the afternoon session covers 5xxx and 6xxx level course material in a greater depth. The morning session covers basic concepts and problems related to computational intelligence related areas. Such topics are covered in courses including: CpE 5310/EE 5310/ Sys Eng 5211 -Computational Intelligence, CpE/EE 4001-Adaptive Devices, Circuits and Systems, EE 5370 -Introduction to Neural Networks & Applications, CpE/EE 6001 - Advanced Neural Networks and Hardware Implementation and CpE /EE 6320 -Adaptive Critic Designs.

Topics related to CpE 5310/EE 5310 (Computational Intelligence) include:
• Artificial Neural Networks (ANNs):
  The Artificial Neuron; Supervised Learning Neural Networks; Unsupervised Learning
Neural Networks; Radial Basis Function Networks. This part will be introductory in nature since most of the course involves EC, SI, and FS methods for training and developing ANN structures.

- **Evolutionary Computing (ECs):**  
  Genetic Algorithms (GAs), Genetic Programming (GP), Evolutionary Programming (EP), Evolutionary Strategies (ESs). Applications of these algorithms (GAs, ESs) to train neural networks will be emphasized.

- **Artificial Immune Systems (AIS):**  
  The biological immune system is a highly parallel and distributed adaptive system. It uses learning, memory, and associative retrieval to solve recognition and classification tasks. Artificial Immune Systems is a new computational approach for the CI community. It is an excellent tool for solving engineering problems. The design of robust controllers using AIS will be covered among other applications.

- **Swarm Intelligence (SI):**  
  Particle Swarm Optimization (PSO); Ant Colony Optimization; Cultural Evolution. Applications of PSO to train neural networks will be emphasized. The integration of Swarm and Cultural evolution will be discussed.

- **Fuzzy Systems (FS):**  
  Fuzzy Systems; Fuzzy Interference Systems; Fuzzy Controllers; Rough Sets.

- **Hybrid Systems:**  
  The integration of these CI paradigms in the development of hybrid systems for solving engineering problems. For example, the application of CI in optimal digital circuits design, mapping and routing on hardware, in design of identifiers and controllers for nonlinear systems, image and signal processing, etc.

**Recommended references:**
- *Computational Intelligence - An Introduction* by A. P. Engelbrecht
- *Computational Intelligence – Concepts to Implementations* by R Eberhart and Y Shi

**Topics related to EE 5370 (Introduction to Neural Networks & Applications) (Prerequisite: Math 3329 or Math 3304 or equivalent) include:**
- **Describe real neural network structures mathematically.**
- **Describe, interpret, and/or apply architectures and techniques, including adaline, madaline, back propagation, BAM, Hopfield memory, counterpropagation networks, self organizing maps, adaptive resonance theory.**
- **Describe a neural network architecture based on a sample problem and data.**

**Recommended references:**
- S Haykin, *Neural Networks*
- Software: Matlab Software and Neural Network Toolbox
Topics related to CpE/EE 4001 (Adaptive Devices, Circuits and Systems) include:

This course will cover EHW concepts for the evolution of devices, circuits and systems. Some of the topics to be covered in this course are listed below but are not limited to:

- Evolutionary and Swarm Algorithms
- Evolvable Hardware (EHW) – Using Evolutionary Computation to Design and Optimize Hardware Systems
- Bio-inspired machines – The Embryonics Approach
- Analog and Digital Hardware Evolution
- Fault Tolerant Sensor and Sensor Networks
- Evolution and Reconfiguration power networks.
- Evolution of Instruments and Devices

Recommended references:

Topics related to CpE 6320/EE 6360 (Adaptive Critic Designs) include:

- Reinforcement learning
- Dynamic Programming (DP) and Approximate Dynamic Programming (ADP)
- Adaptive critics
  - Class of Adaptive Critics
  - Heuristic Dynamic Programming (HDP) and Action Dependent HDP
  - Dual Heuristic Programming (DHP)
  - Global Dual Heuristic Programming (GDHP)

Recommended references:

Topics related to CpE/EE 6001 (Advanced Neural Networks and Hardware Implementation) include:

- Recurrent network architectures
- Hopfield neural network - Energy function, Hebbian learning, stability analysis
- Recurrent multilayer perceptron - recurrent learning algorithms, time series modeling and prediction, control and speech applications.
- Neural Network Hardware (NNHW)
  1. Overview
     - Why Hardware
     - NNHW Applications
- Hardware vs. Software
- Designer's Dilemma
- User's Dilemma
- NNHW Applications

2. NNHW
- Introduction
  - a. Chips
    - i. Digital
    - ii. Analog & Hybrids
    - iii. Neuromorphic
  - b. General vs. Specialized Hardware
  - c. NNHW Systems
    - i. Neurocomputers
    - ii. Accelerator cards

Recommended references:
- *Text for hardware implementations to be added.*

The morning session will cover all 5xxx level course materials and the afternoon session will cover 5xxx and 6xxx level course material in a greater depth.

5. Networking

The morning session covers basic concepts and problems related to networked systems. Such topics are covered in courses including CpE 5410, Digital Network Design and CpE 5420 Trustworthy, Survivable Computer Networks.

Topics related to networking include:
- Interpret and design network architectures
- Describe the fundamentals of a layered network architecture model. Show the transfer of information, from source to destination, through gateways, routers, or bridges.
- Describe the basic protocols of the TCP/IP suite.
- Describe the functioning of a firewall and/or a Virtual Private Network (VPN)
- Discuss commonalities and differences between wired and wireless networks
- Discuss basic security and reliability issues in networking
- Discuss various networking standards

Recommended references:

The afternoon area will cover the same material as the morning session, though in greater depth and with greater emphasis on security and fault-tolerance.
6. Security and Reliability

The morning session covers basic concepts and problems related to computer and network security and reliability. Such topics are covered in courses like CpE 5510, Fault-Tolerant Digital Systems, CpE 5410, Digital Network Design and CpE 5420 Trustworthy, Survivable Computer Networks.

Topics related to security include:
- Describe the basic notions of confidentiality, authentication, integrity, and non-repudiation
- Discuss each of the following threats: man-in-the-middle attack, meet-in-the-middle attack, replay attack
- Describe each of the attacks on information flow: interruption, interception, modification, and fabrication, with examples of each
- Describe the typical “life-cycle” of a virus
- Explain the differences between security policies, mechanisms, and services
- Describe the functioning of a firewall and/or a Virtual Private Network (VPN)

Topics related to reliability include:
- Describe advantages of fault-tolerant systems and basic approaches
- Describe redundancy and voting techniques
- Describe recovery and rollback techniques
- Given input, determine MTTR, MTBF, MTTF
- Generate a fault tree analysis from data

Recommended references:
- Reliability of Computer Systems and Networks, Shooman, Wiley
- Security Engineering, Anderson, Wiley

The afternoon area will cover the same material as the morning session, though in greater depth and with greater emphasis on security and fault-tolerance.

7. Electrical Engineering

Please refer to the guidelines for the EE Qualifying exam for additional information about these topics.
8. Computer Science

This area is offered only in the morning session and covers basic concepts and problems related to data structures and algorithms. Such topics are covered in courses including CS 1570 - Introduction to Computer Science, CS 1200 – Discrete Mathematics, CS 1510 - Data Structures, and CS 2500 - Data Structures II.

Topics related to data structures and algorithms include:

- Design and interpret algorithms using various abstract data types such as lists, stacks, queues, and trees
- Algorithm design; algorithm analysis; algorithm correctness; recurrences; dynamic programming; greedy algorithms; spanning tree and shortest path algorithms; maximum flow
- Formal logic; sets, combinatorics, and probability; relations, functions, and matrices; graphs and graph algorithms; modeling arithmetic, computation, and languages

Recommended references:

- W. Stallings, Operating Systems, 5th edition, Addison-Wesley
- A. Robbins, Linux Programming by Example, Prentice Hall